

FIG. 1A

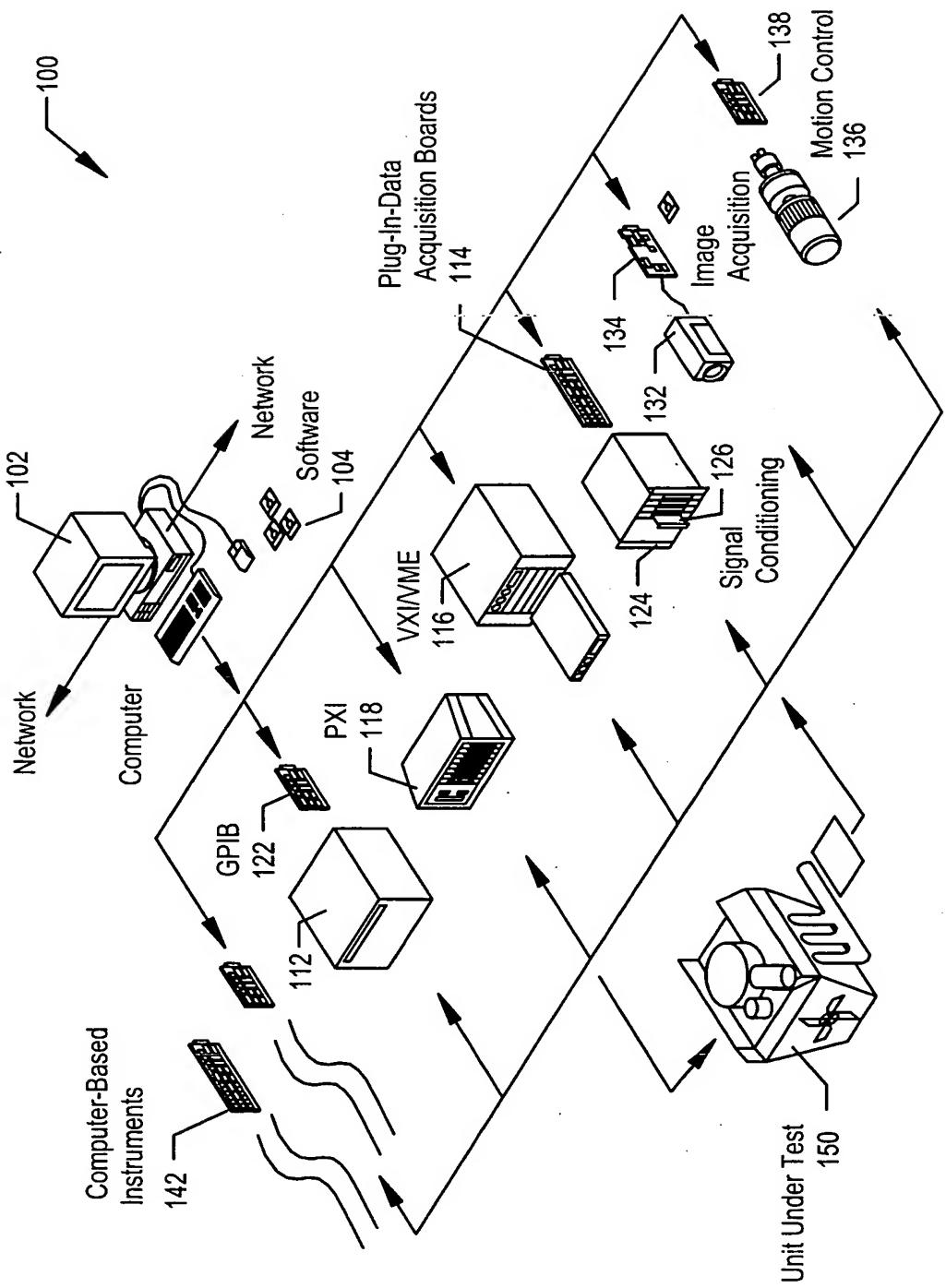
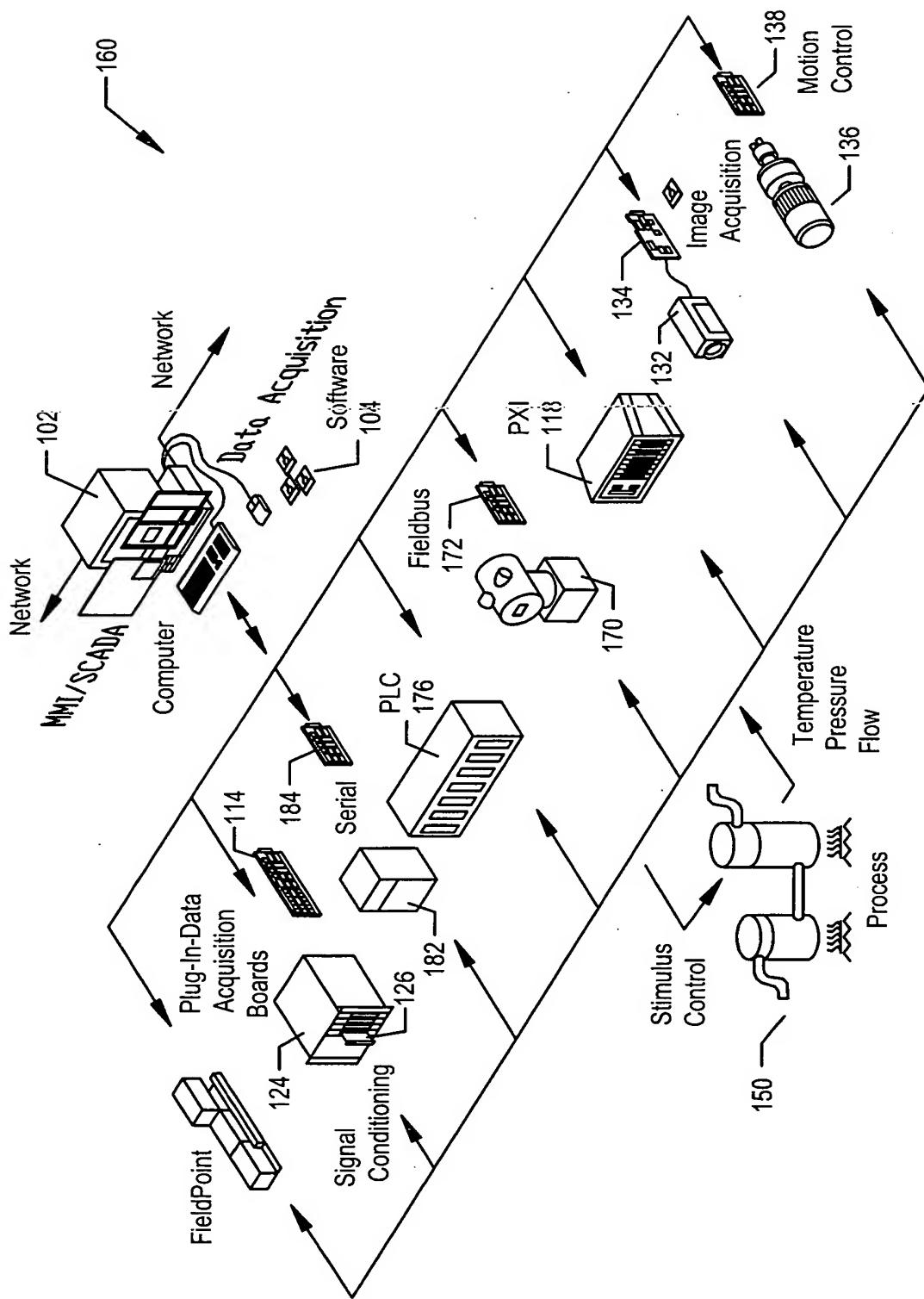


FIG. 1B



12

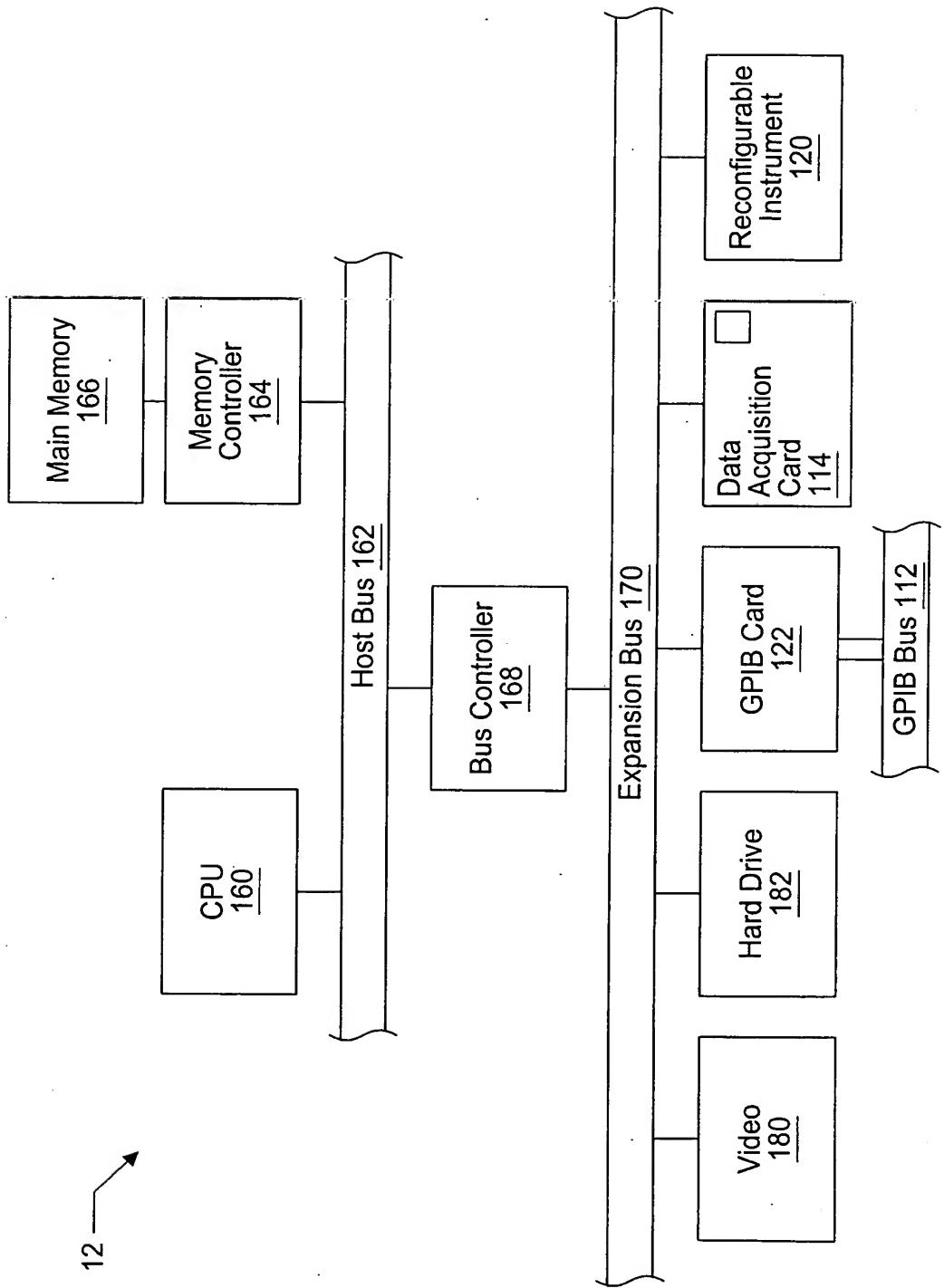


Figure 2

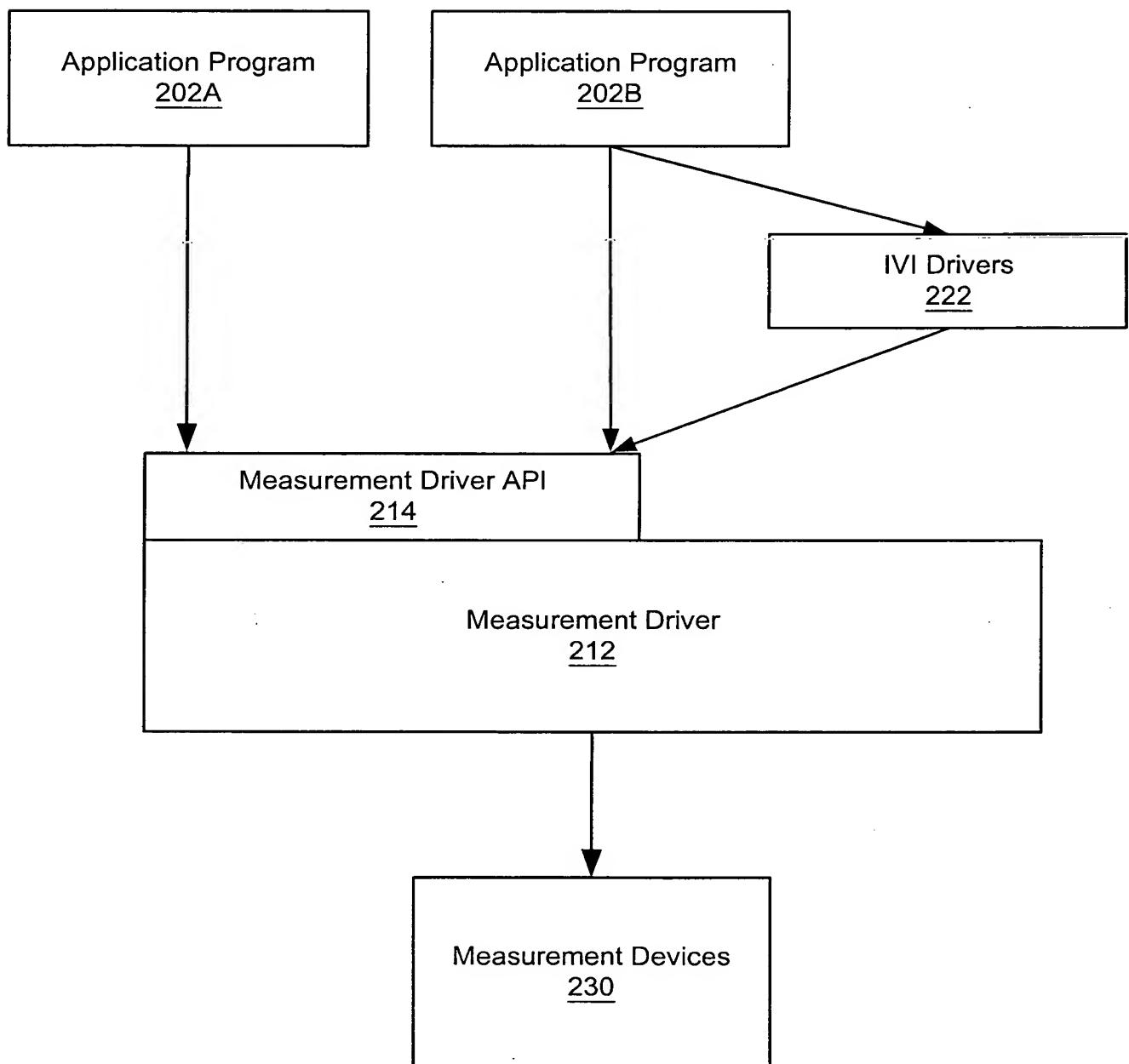


Figure 3

Figure 4

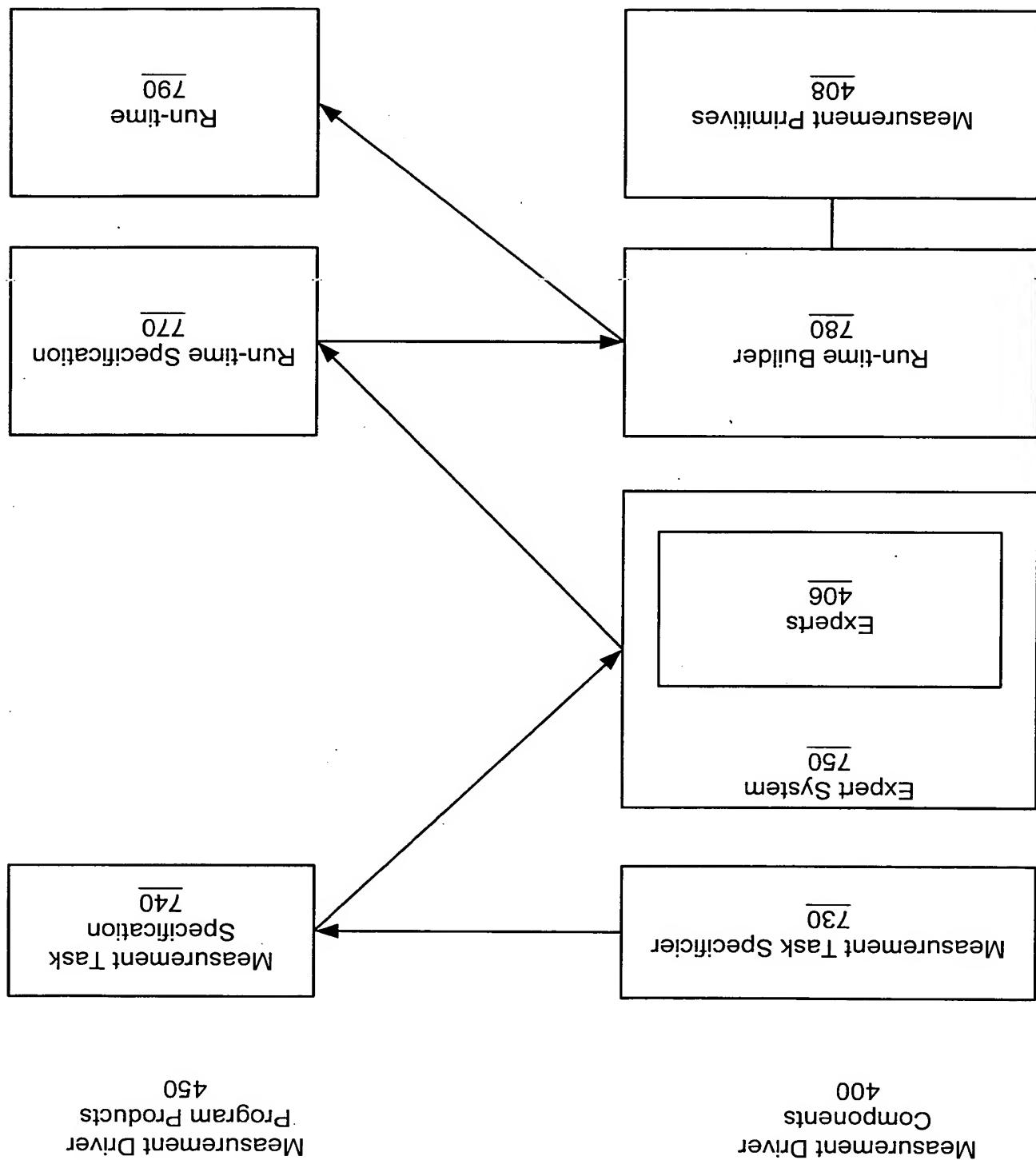
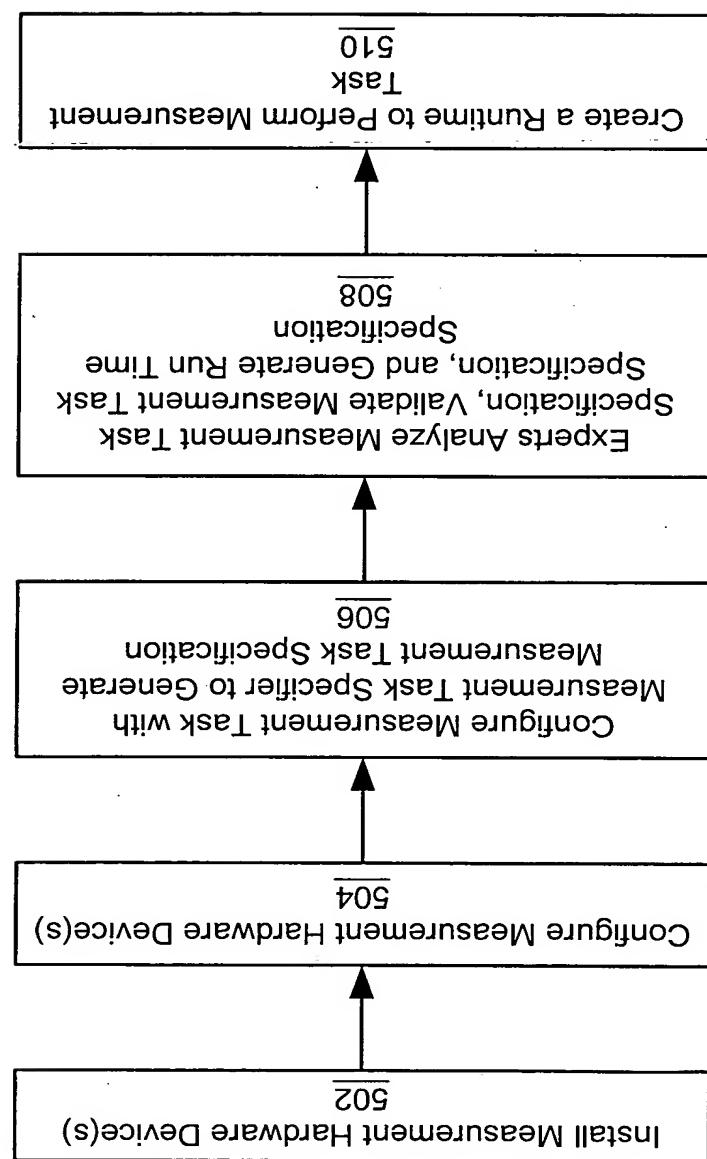
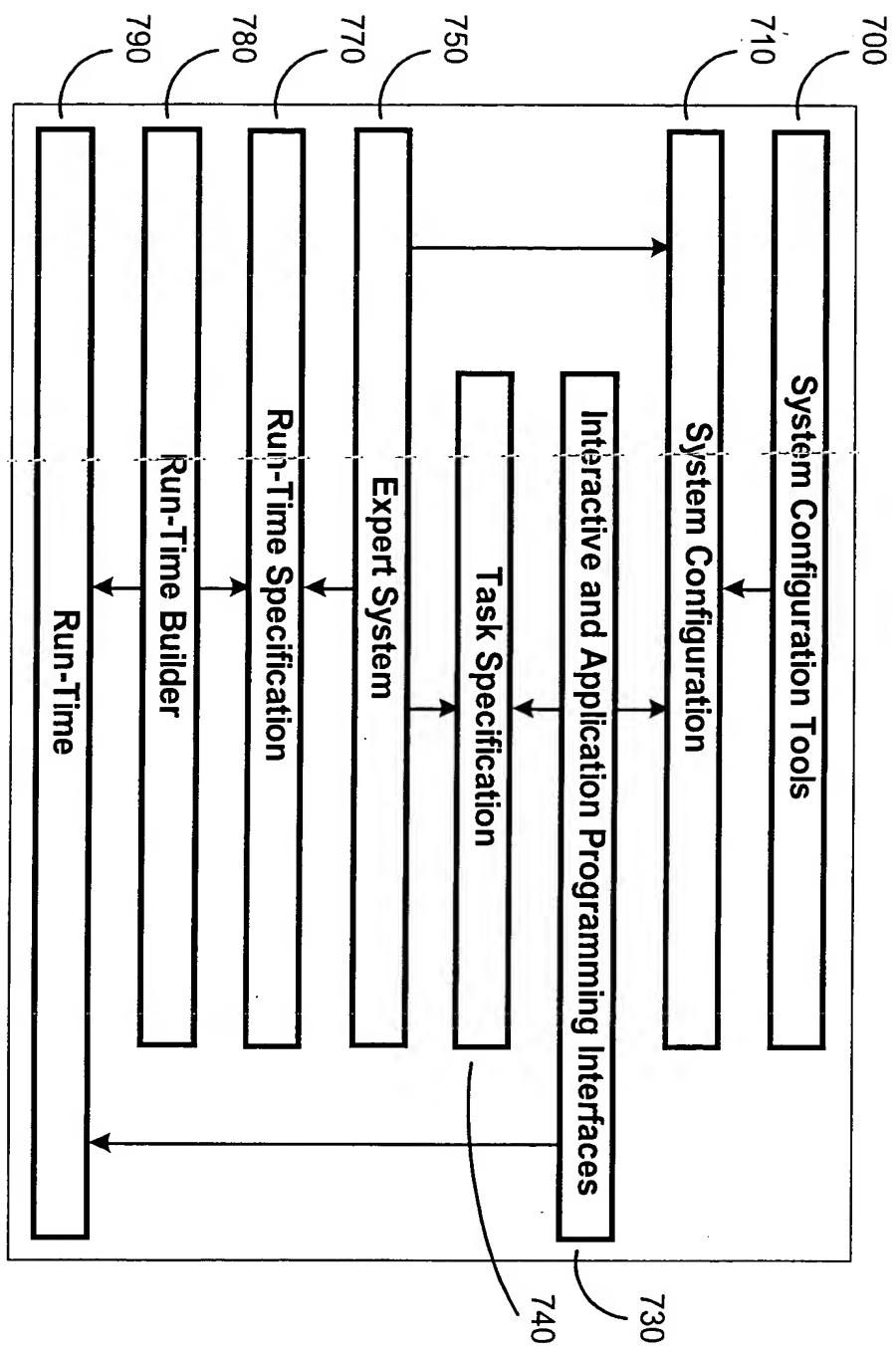


Figure 5





High-Level Architecture

Figure 6

System Configuration and Task Specification

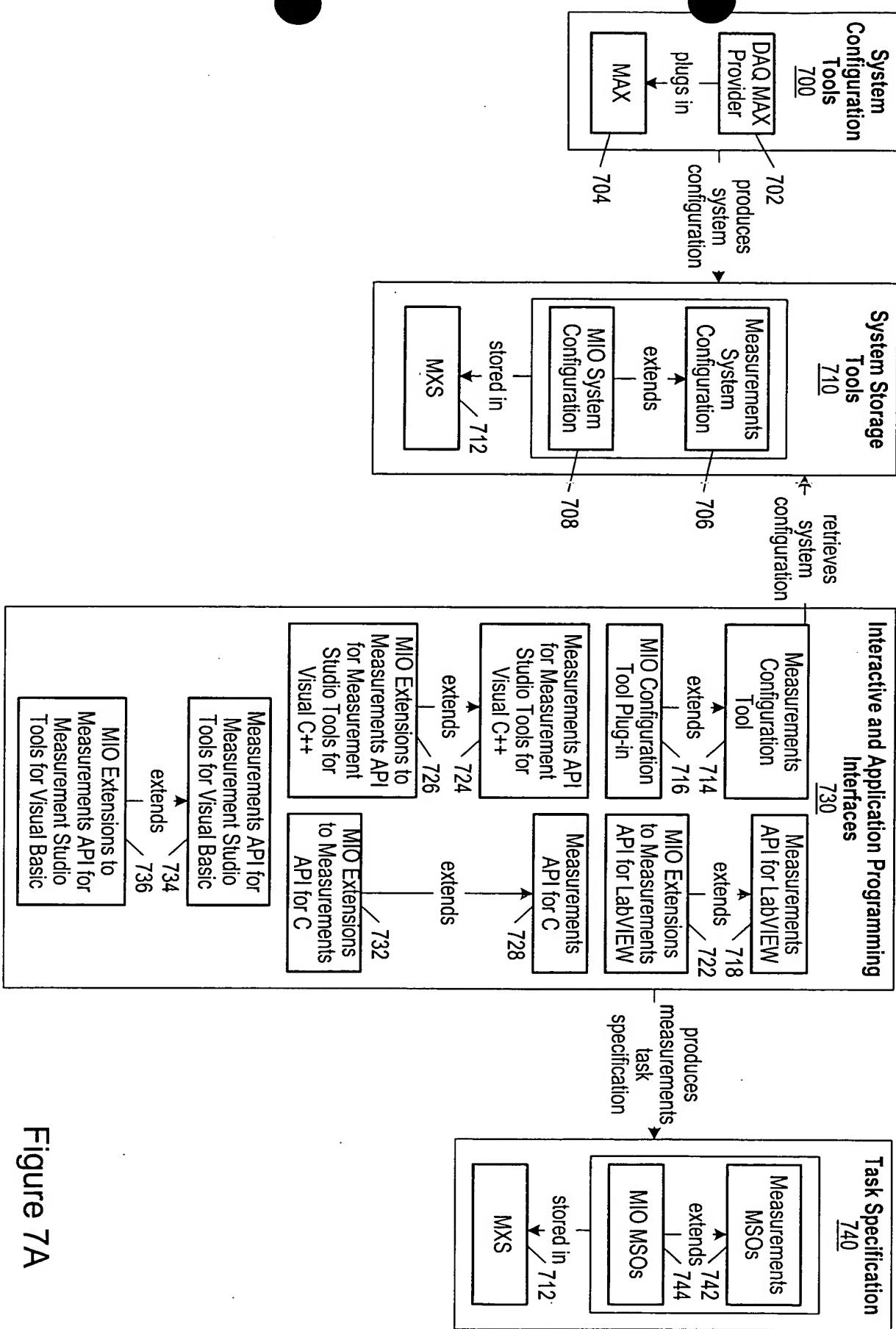


Figure 7A

Compiling Task Specification to Task Run-time Specification

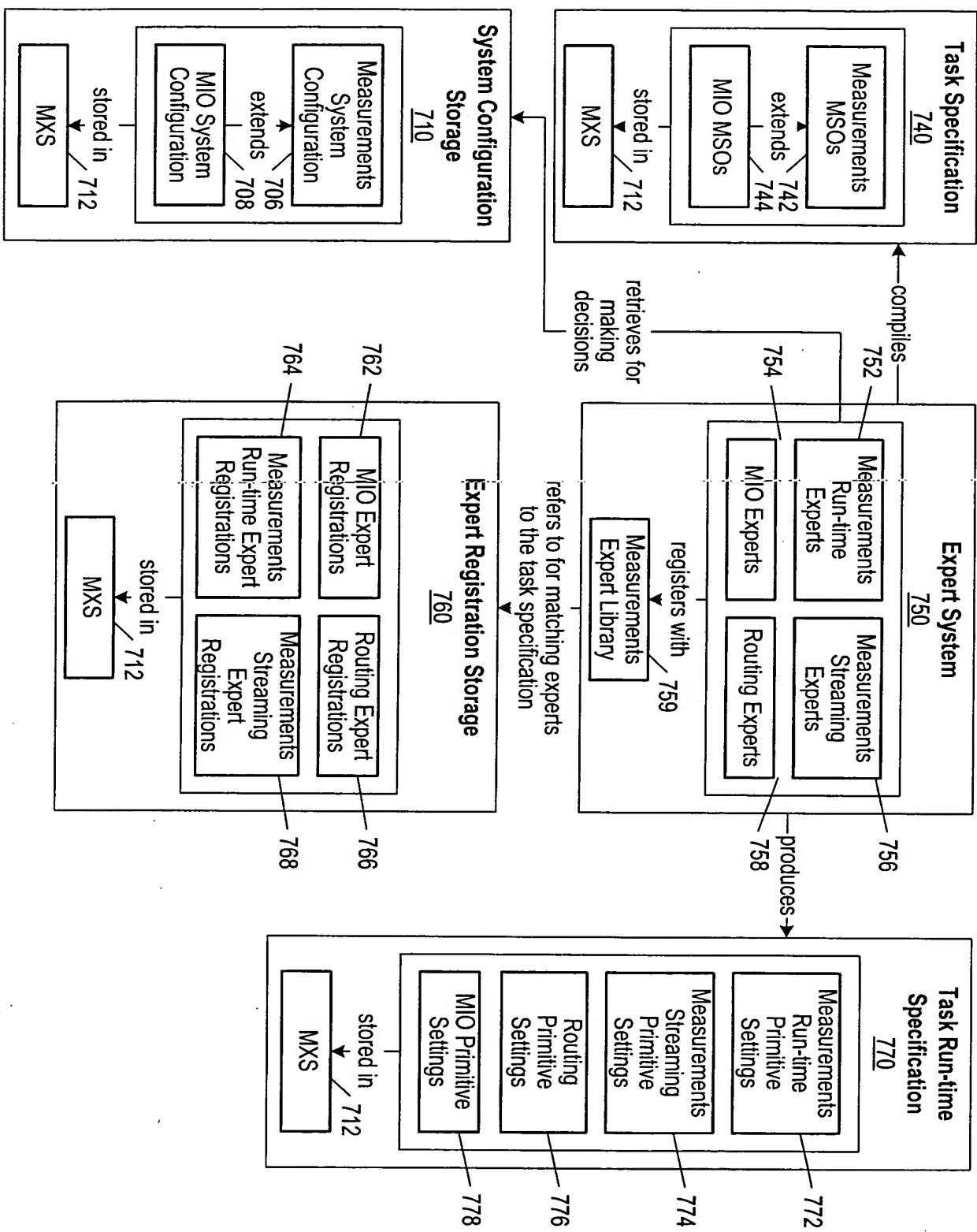


Figure 7B

卷之三

Building Task Run-time from Task Run-time Specification

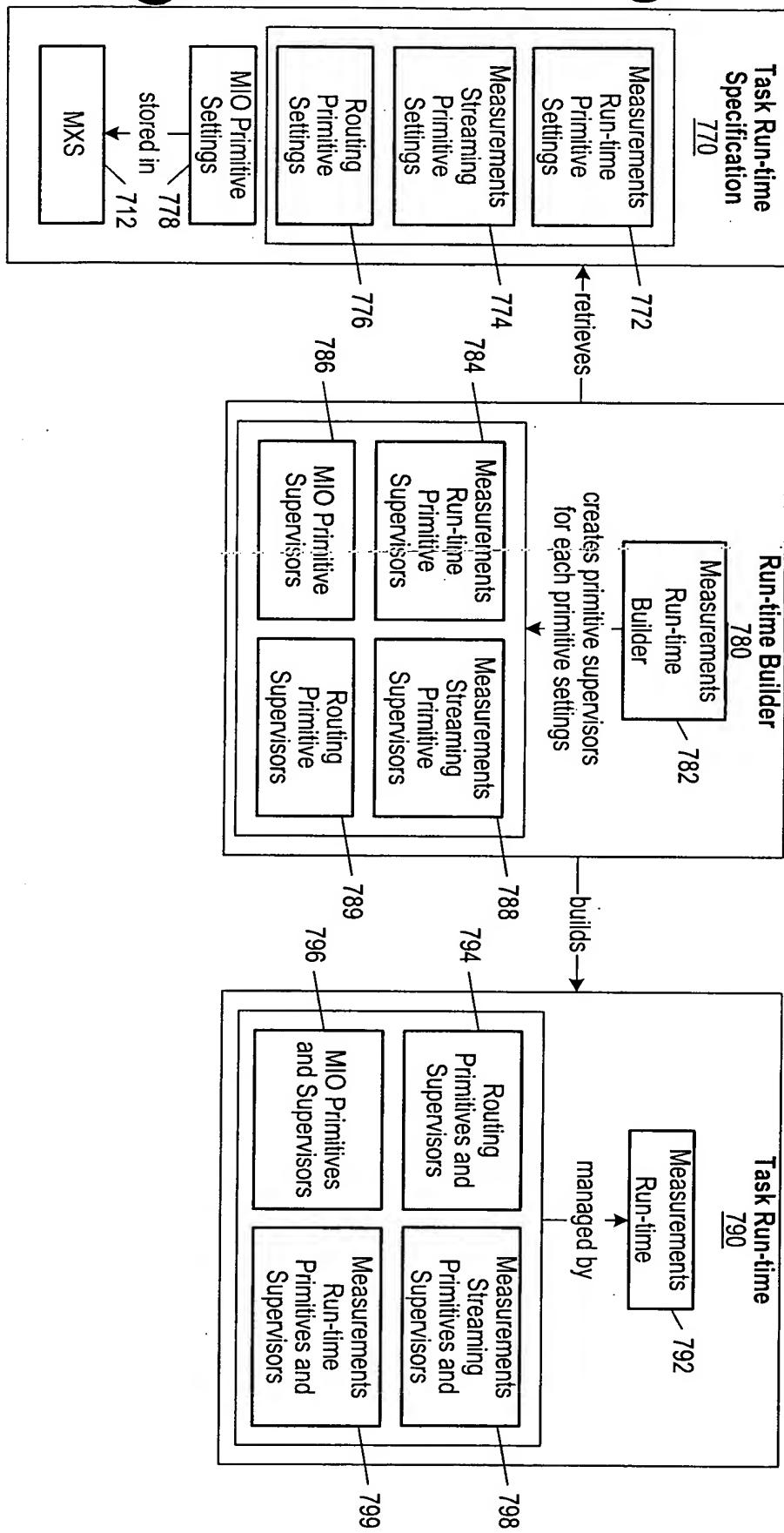


Figure 7C

Executing Tasks

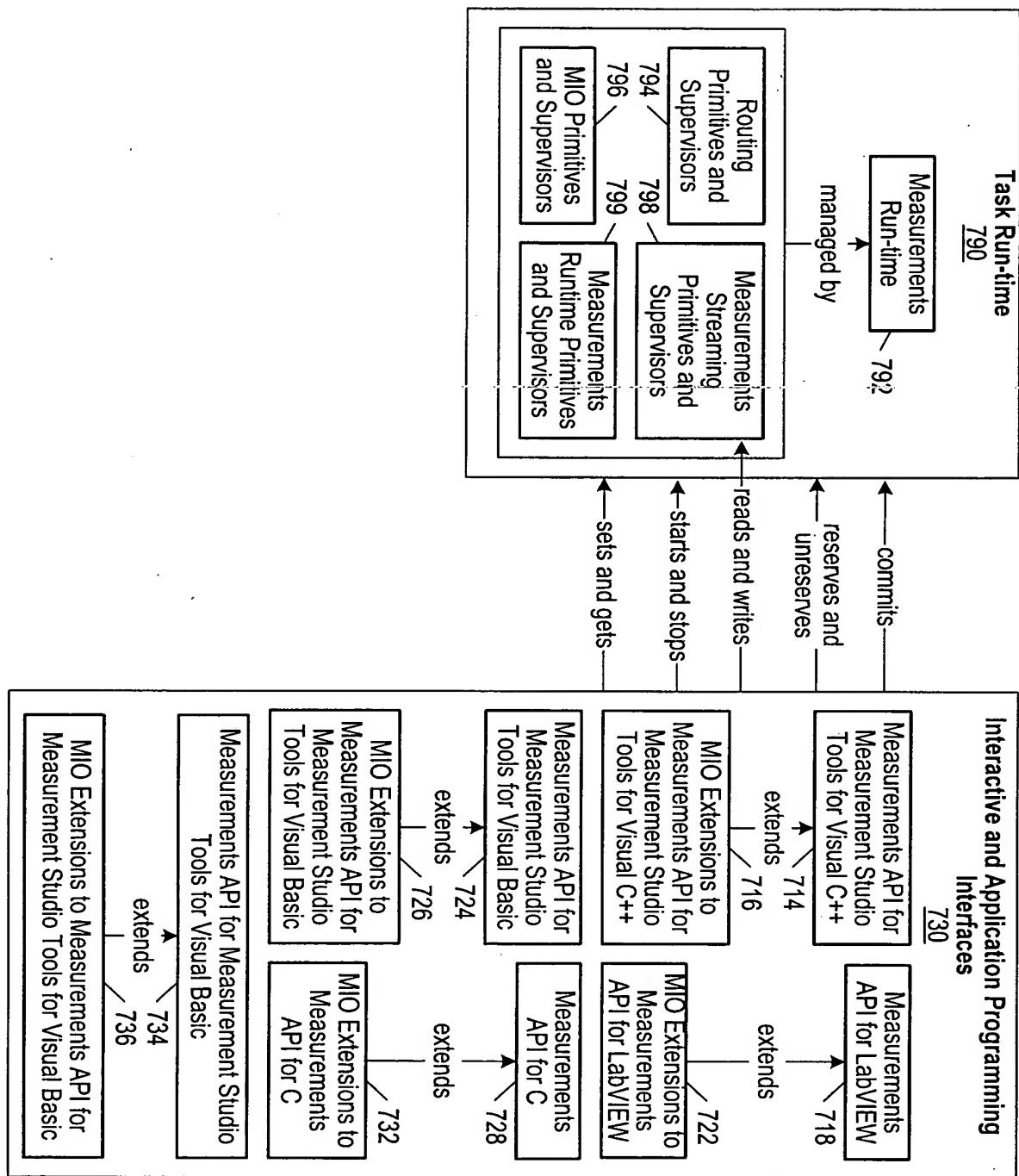


Figure 7D

Packages for System Configuration and Task Specification

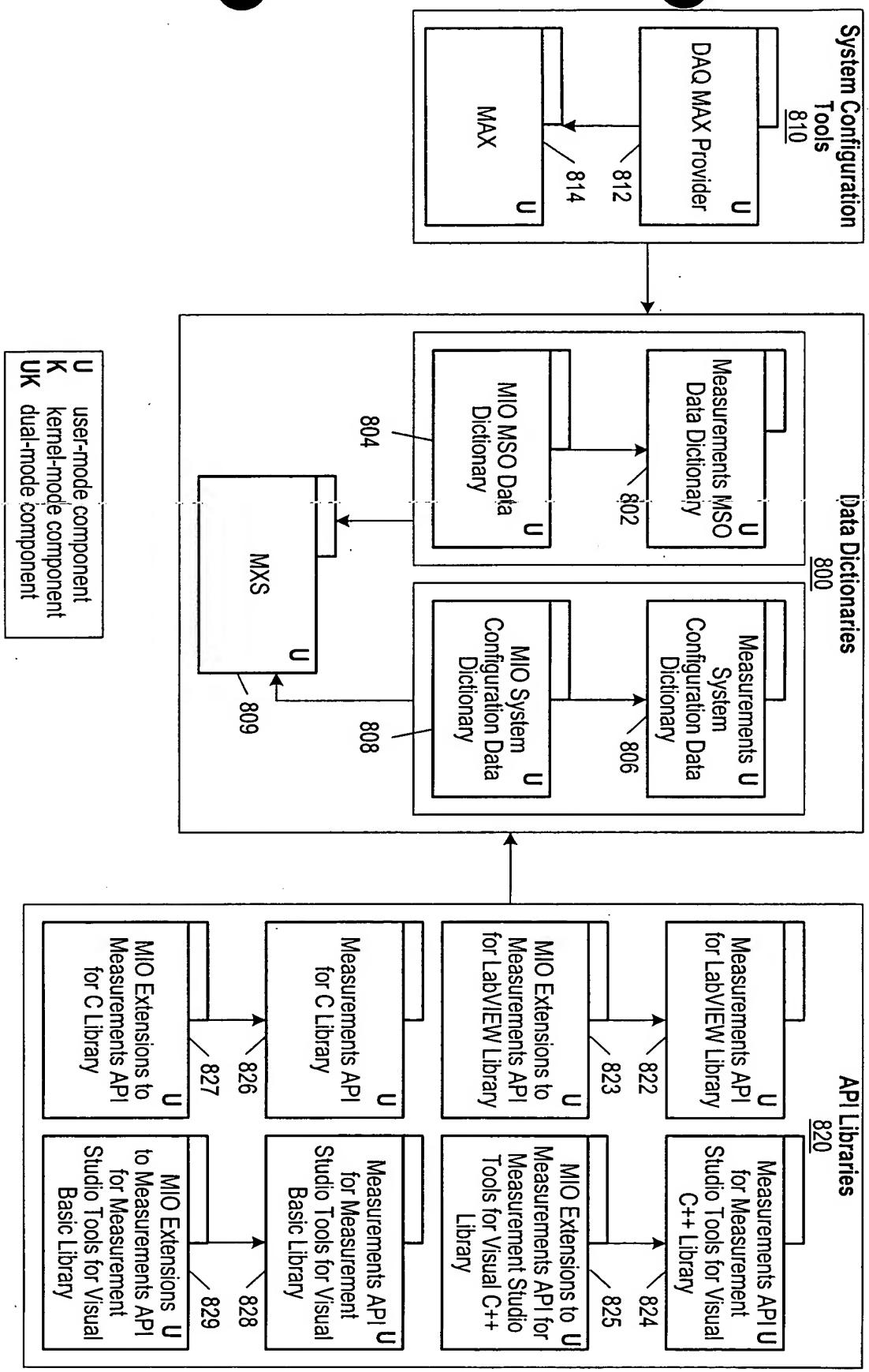


Figure 8A

Packages for Compiling Task Specification to Run-time Specification

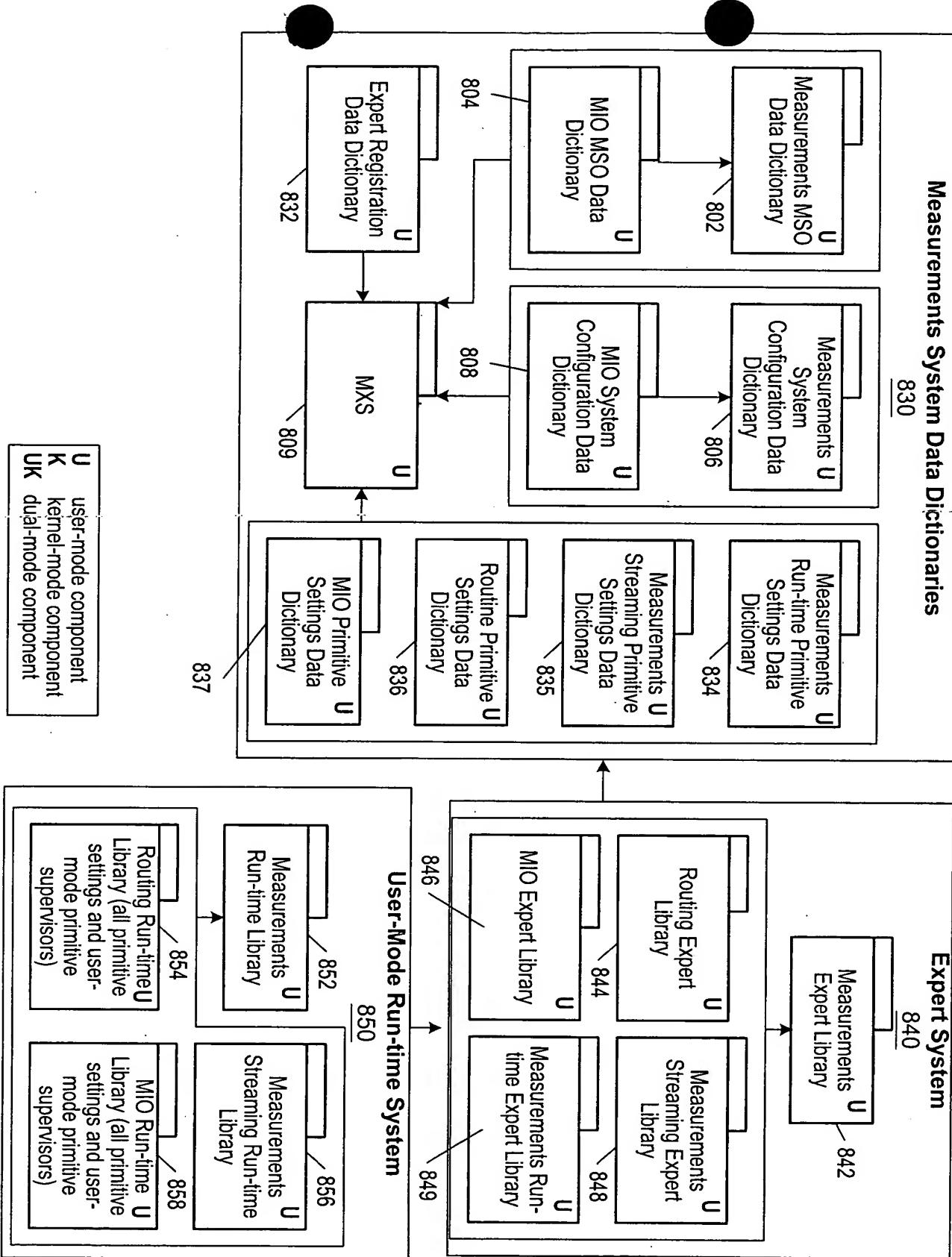


Figure 8B

Packages for Building Task Run-time from Run-time Specification

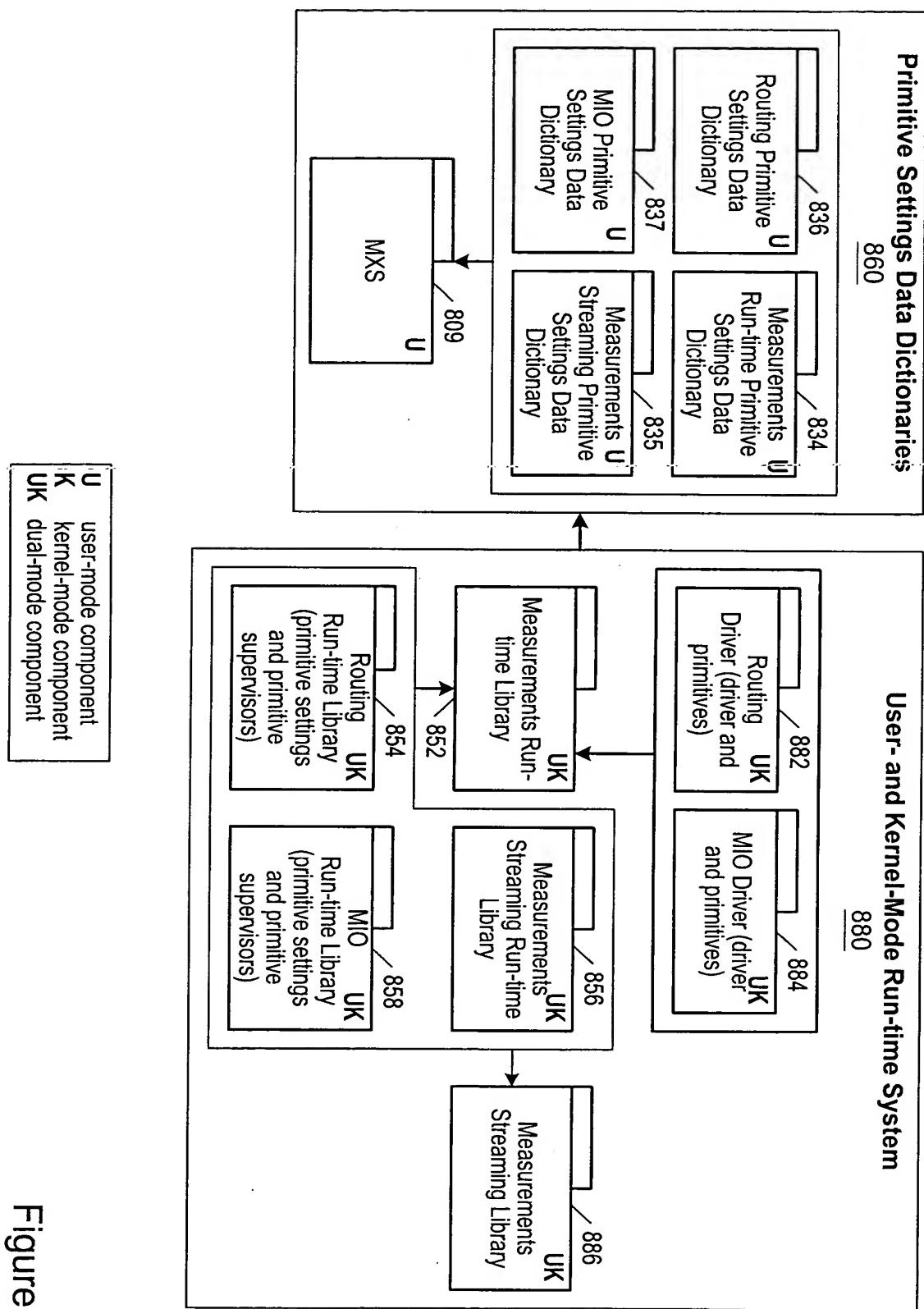


Figure 8C

Packages for Executing Task Run-time

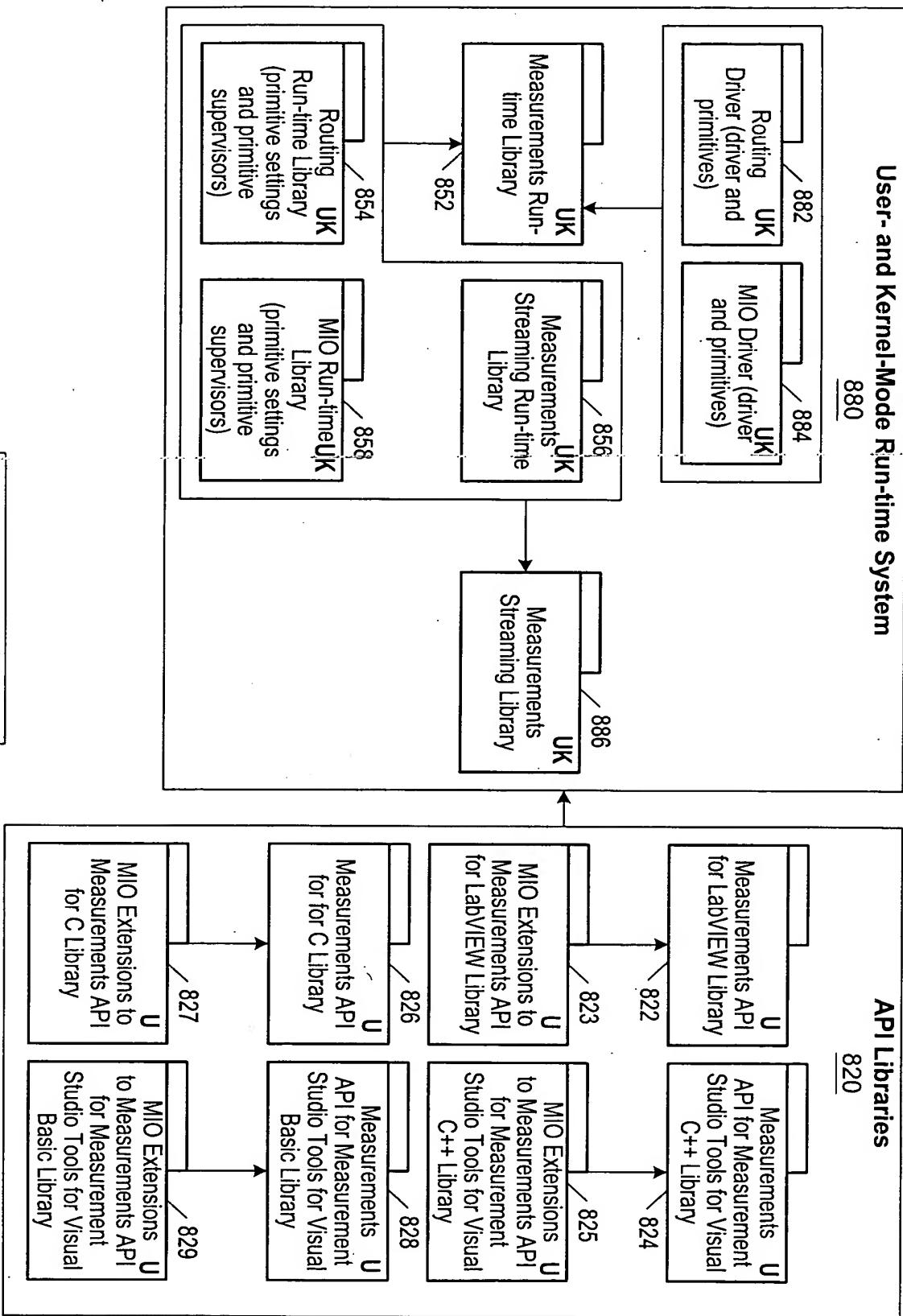


Figure 8D

State Diagram for Measurement Tasks

The Constructed state corresponds to the state of the task at the end of the "Building Task Run-Time from Task Run-Time Specification" static diagram.

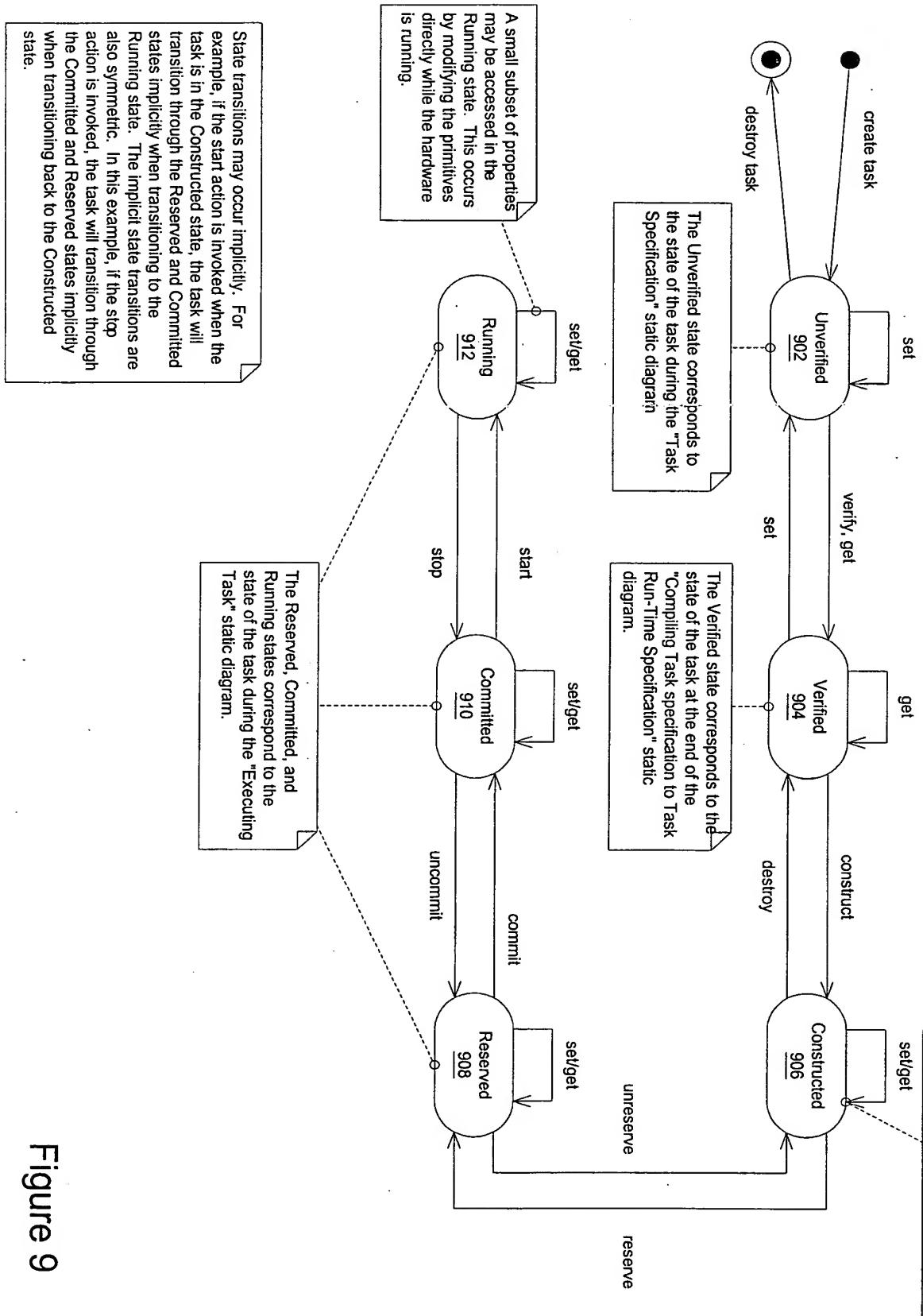


Figure 9

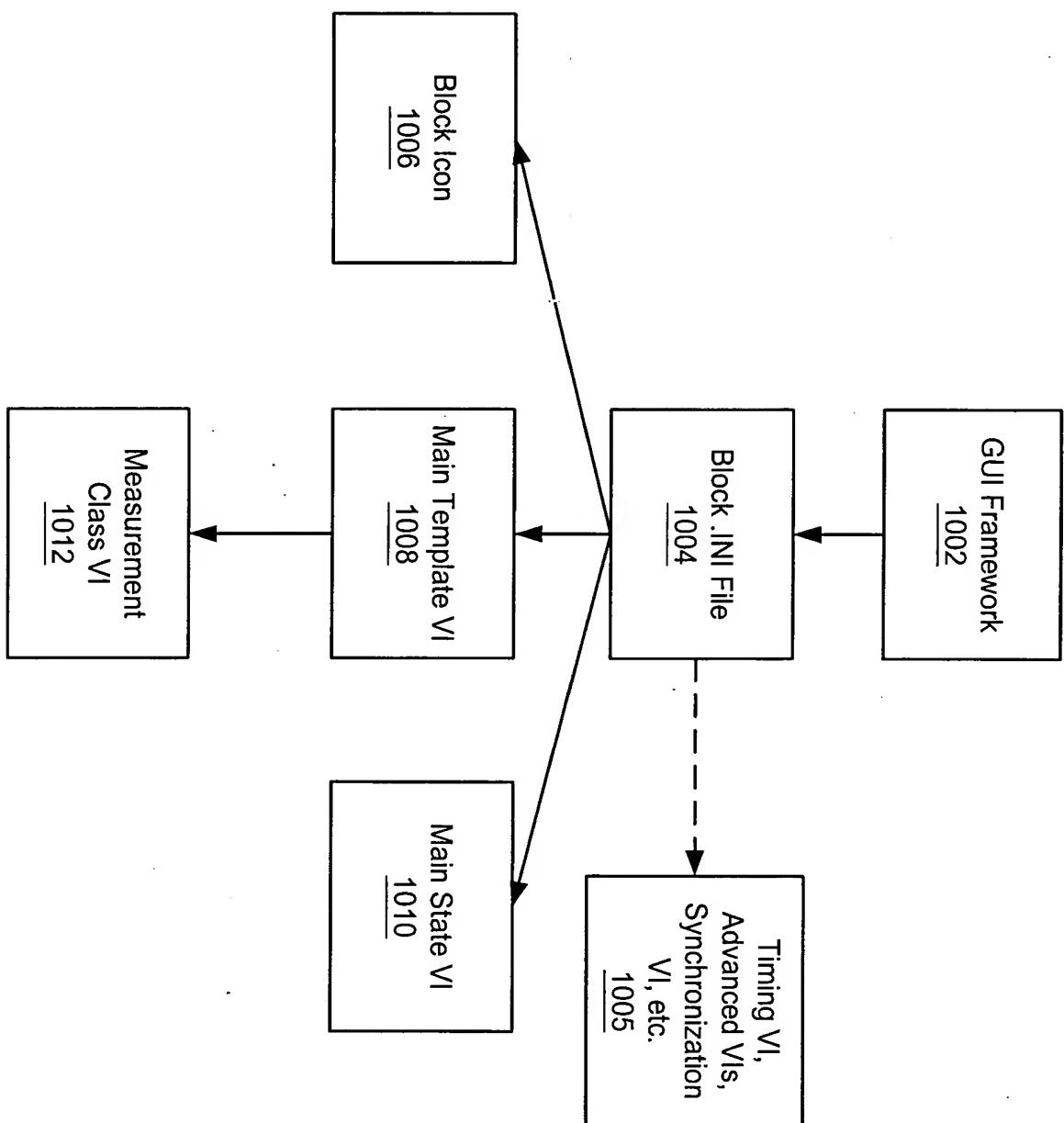


Figure 10

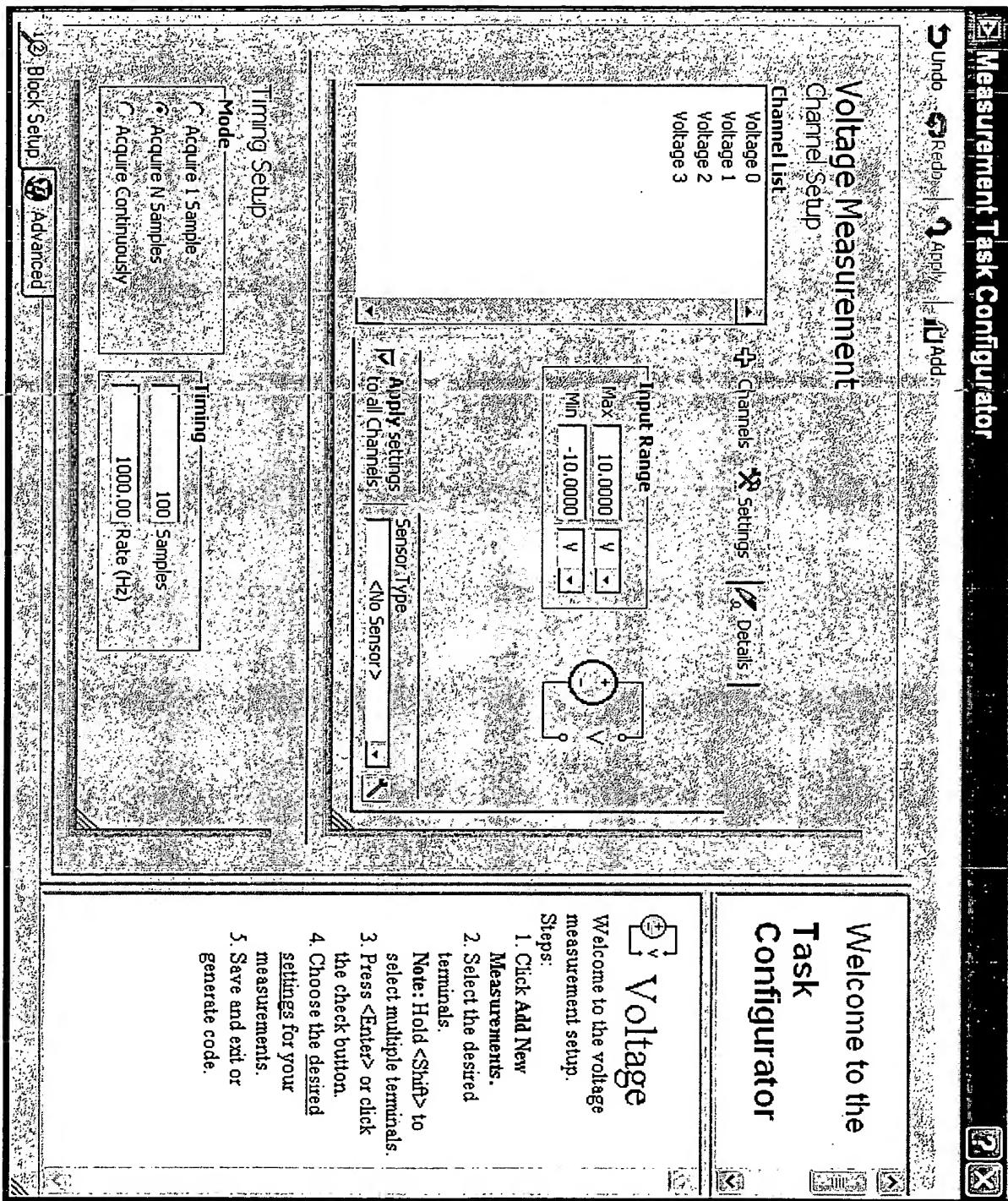


Figure 11

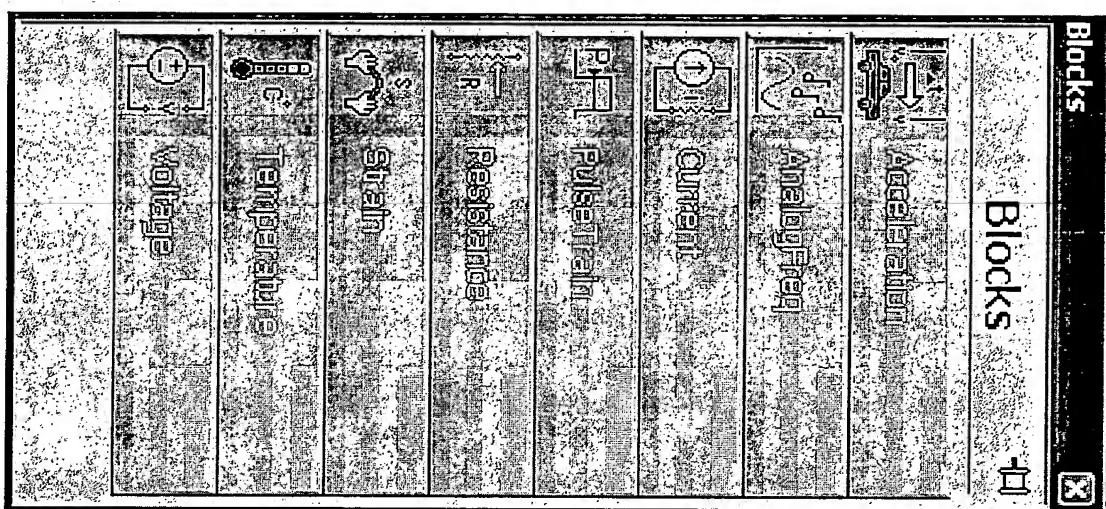


Figure 12A

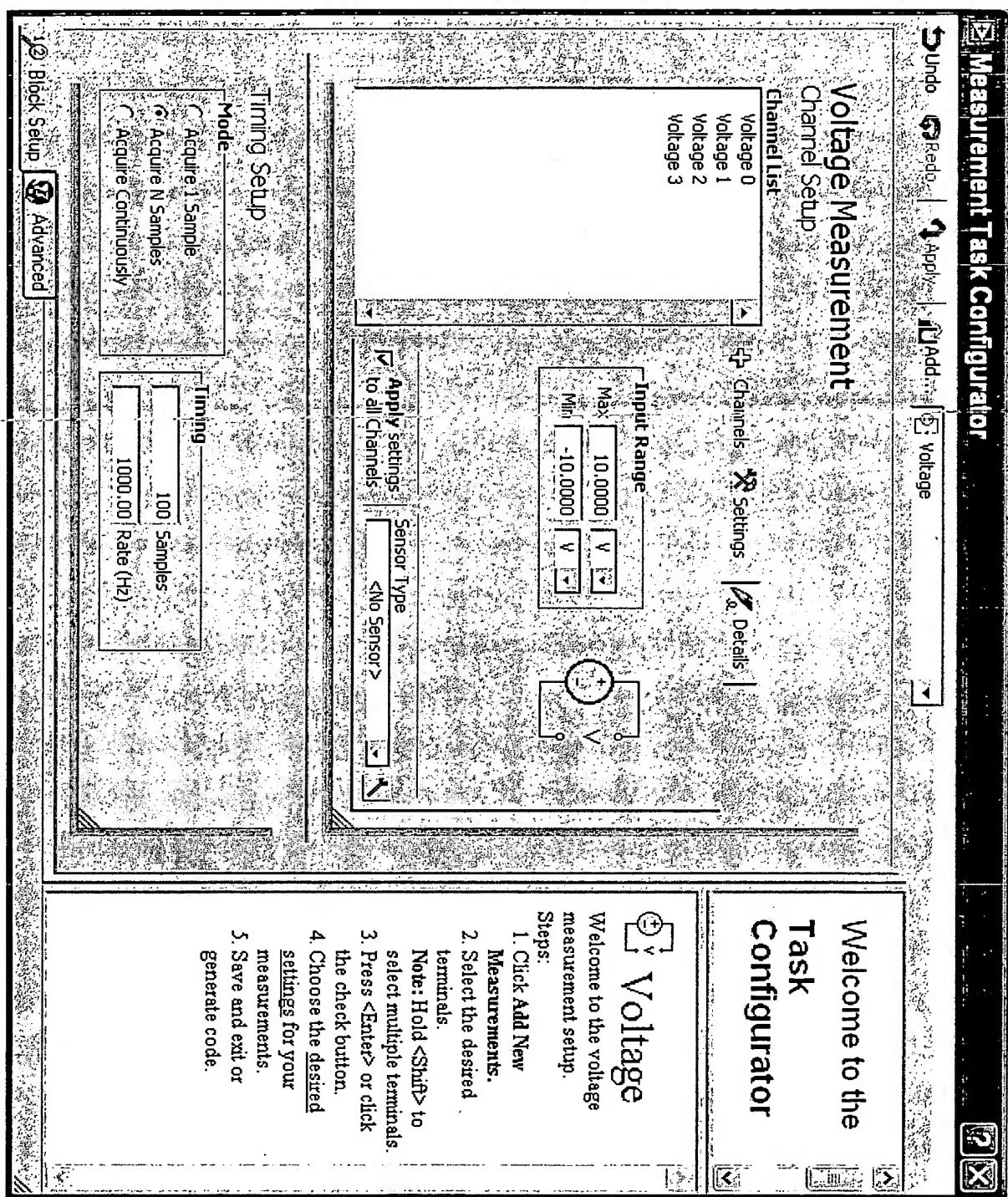


Figure 12B

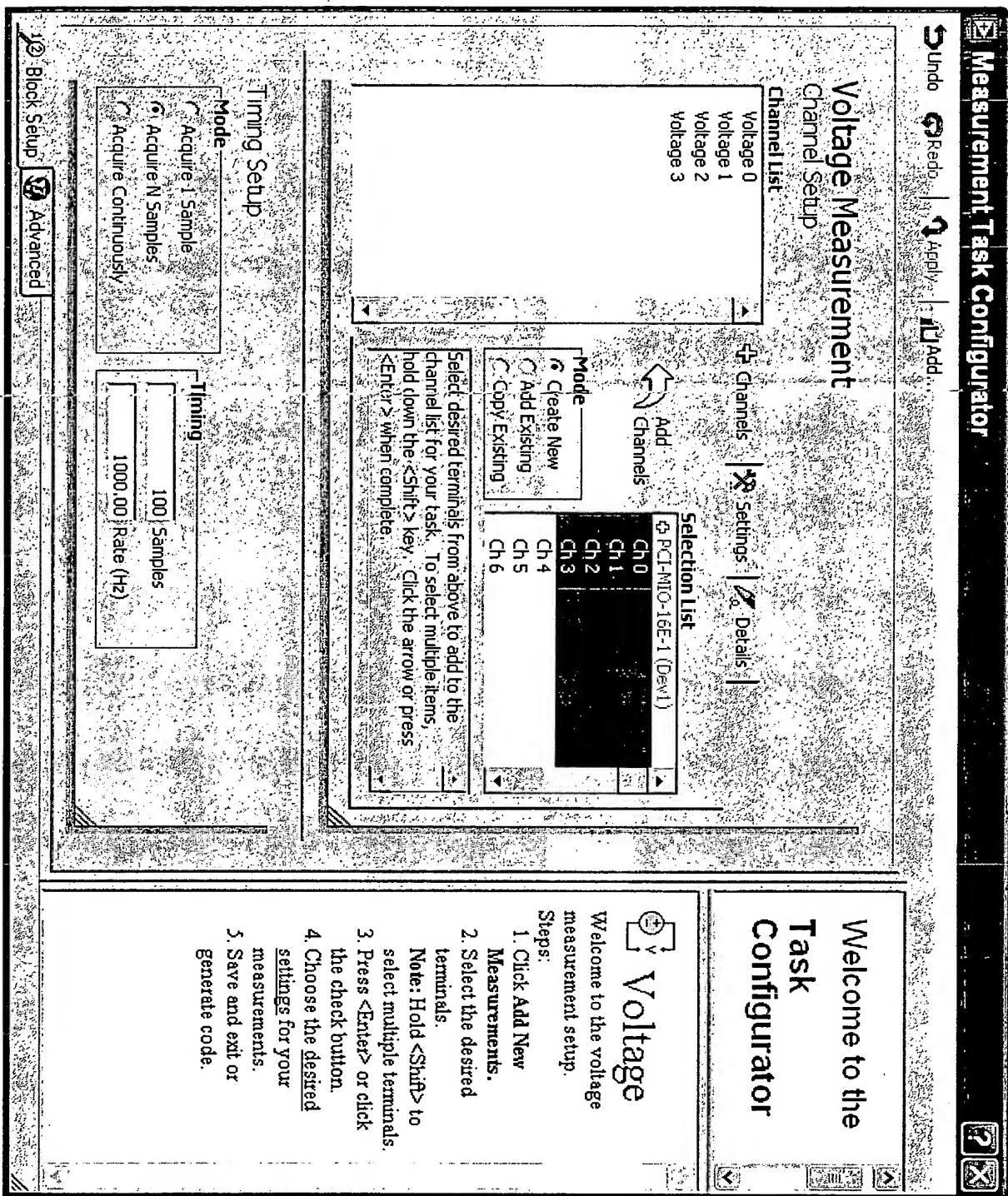


Figure 12C

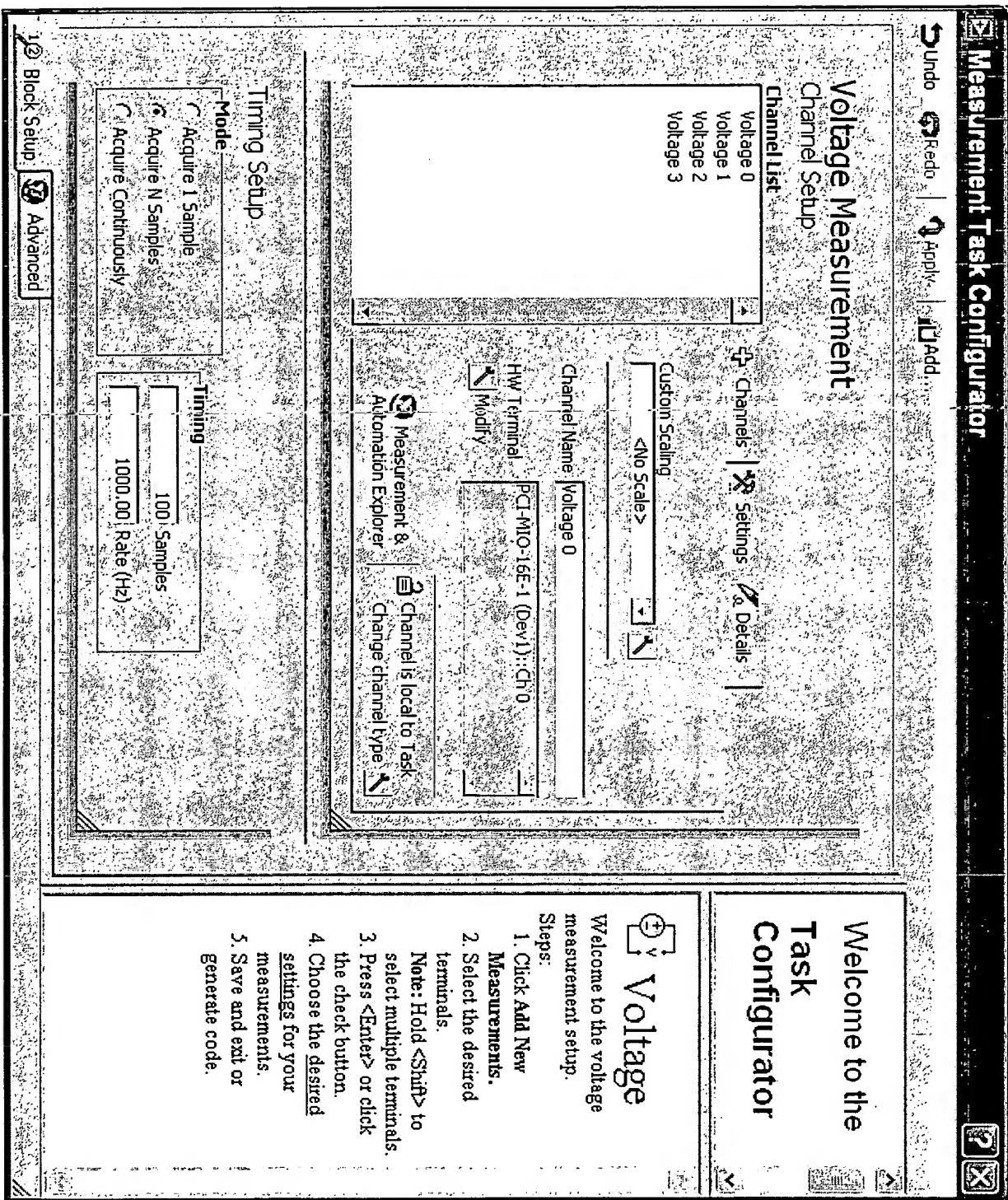


Figure 12D

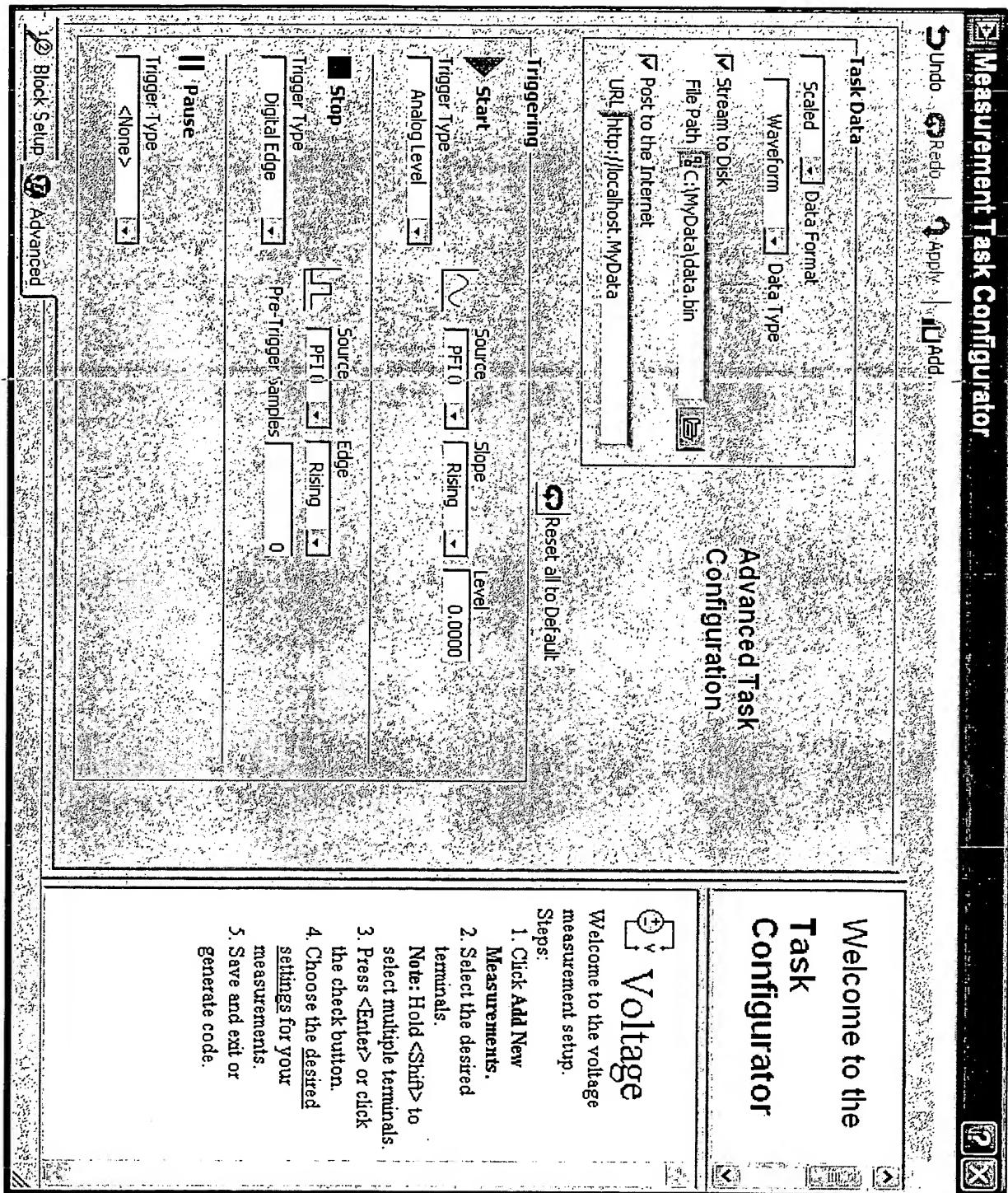


Figure 13

Figure 14

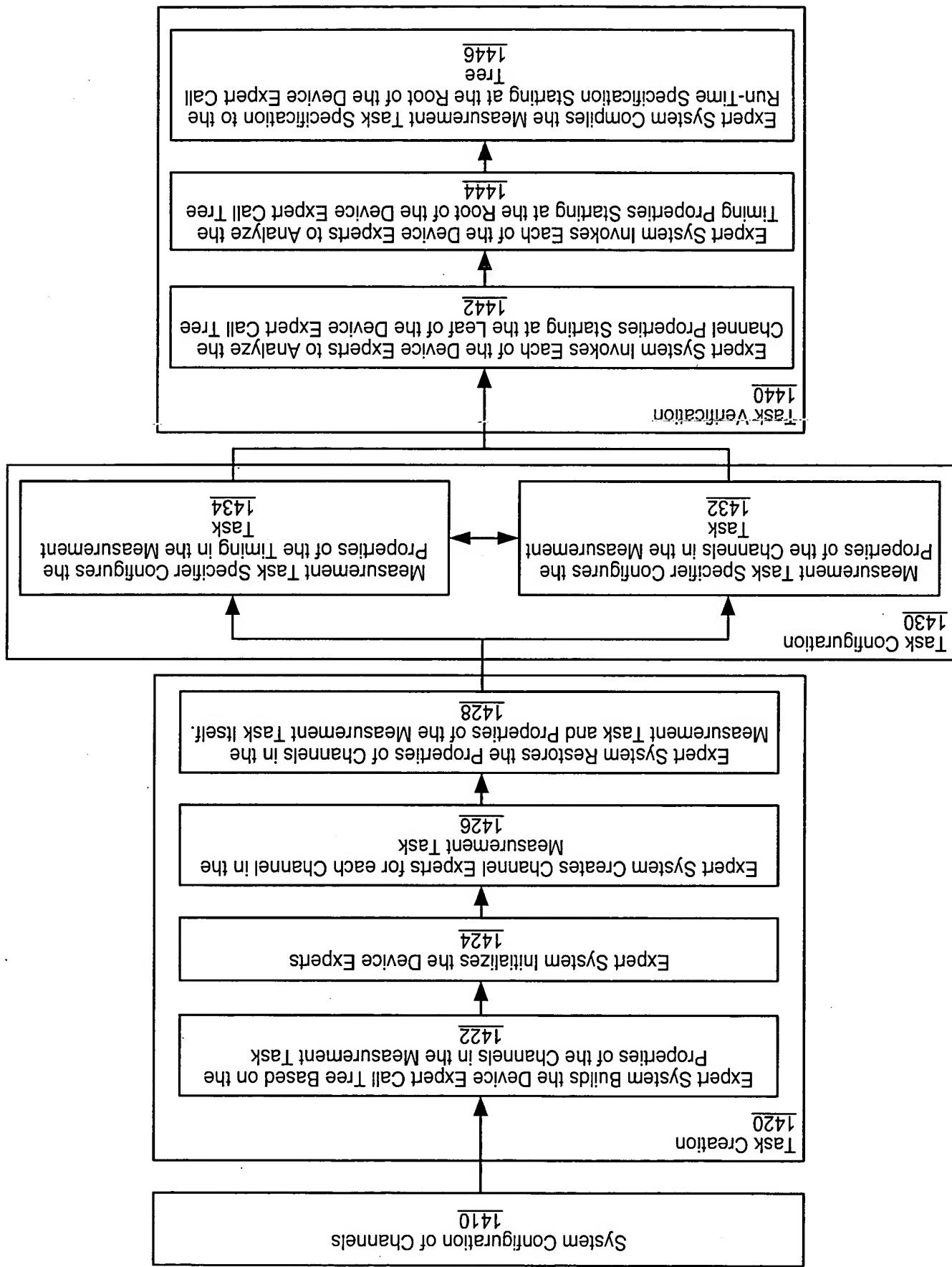
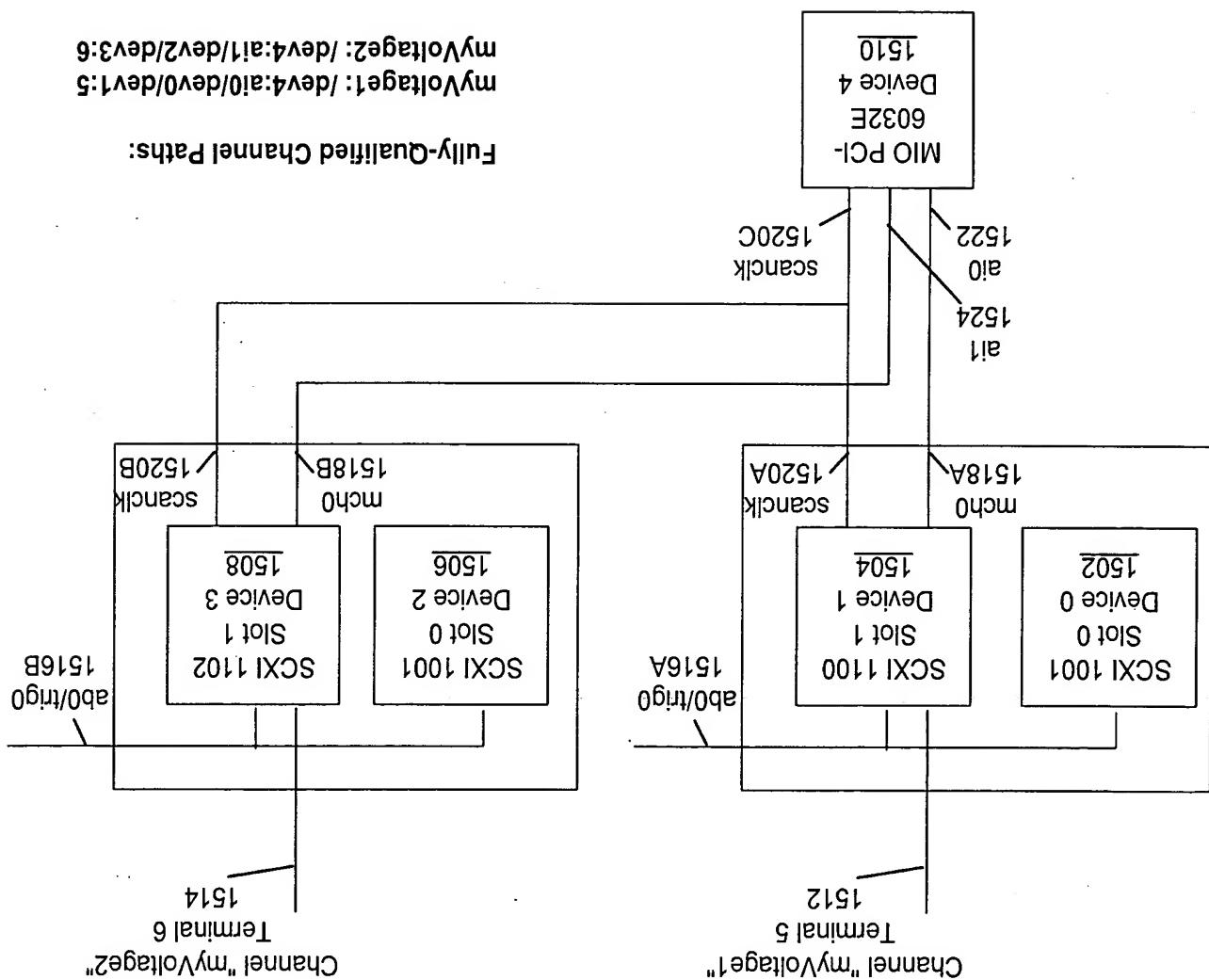
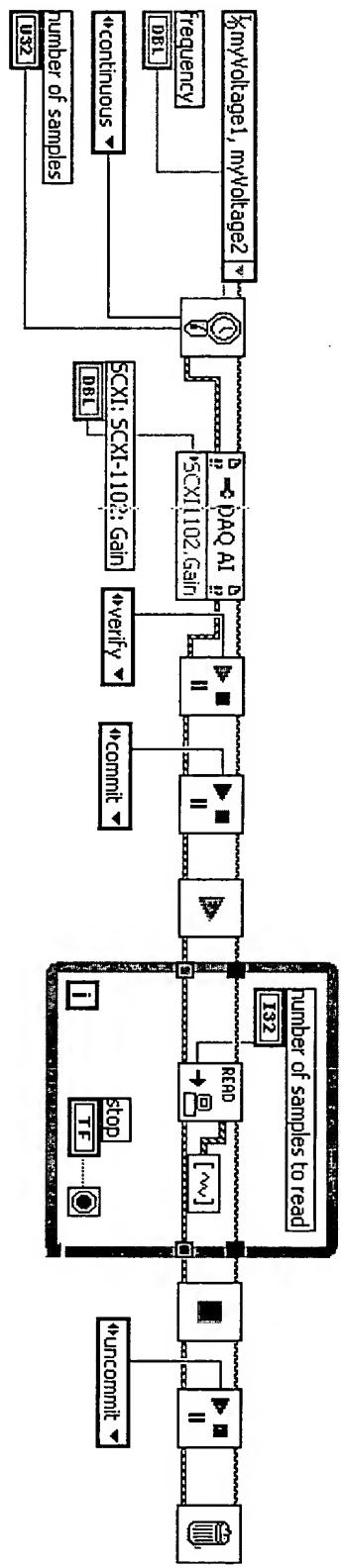


Figure 15

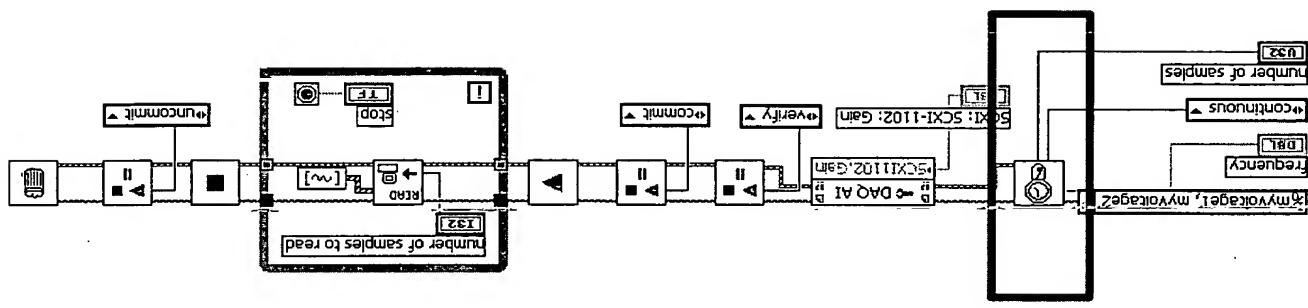




Voltage On Two Channels with Two SCXI Modules in Two
SCXI Chassis Connected to an MIO DAQ Device

Figure 16

Figure 17



Create Device Expert Call Tree

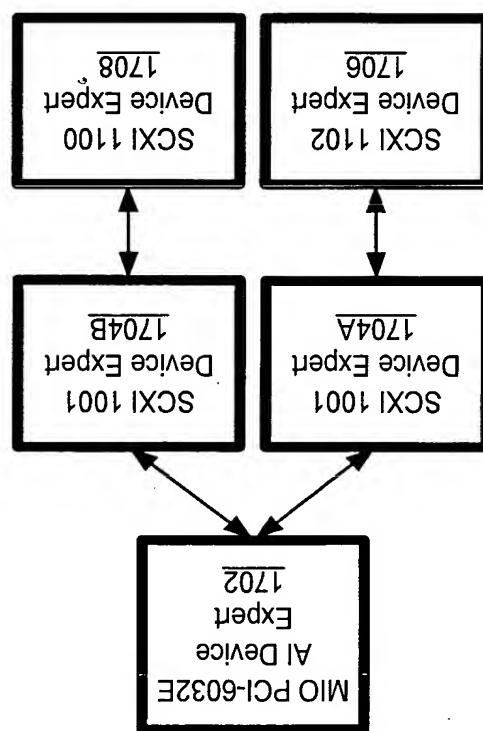


Figure 18

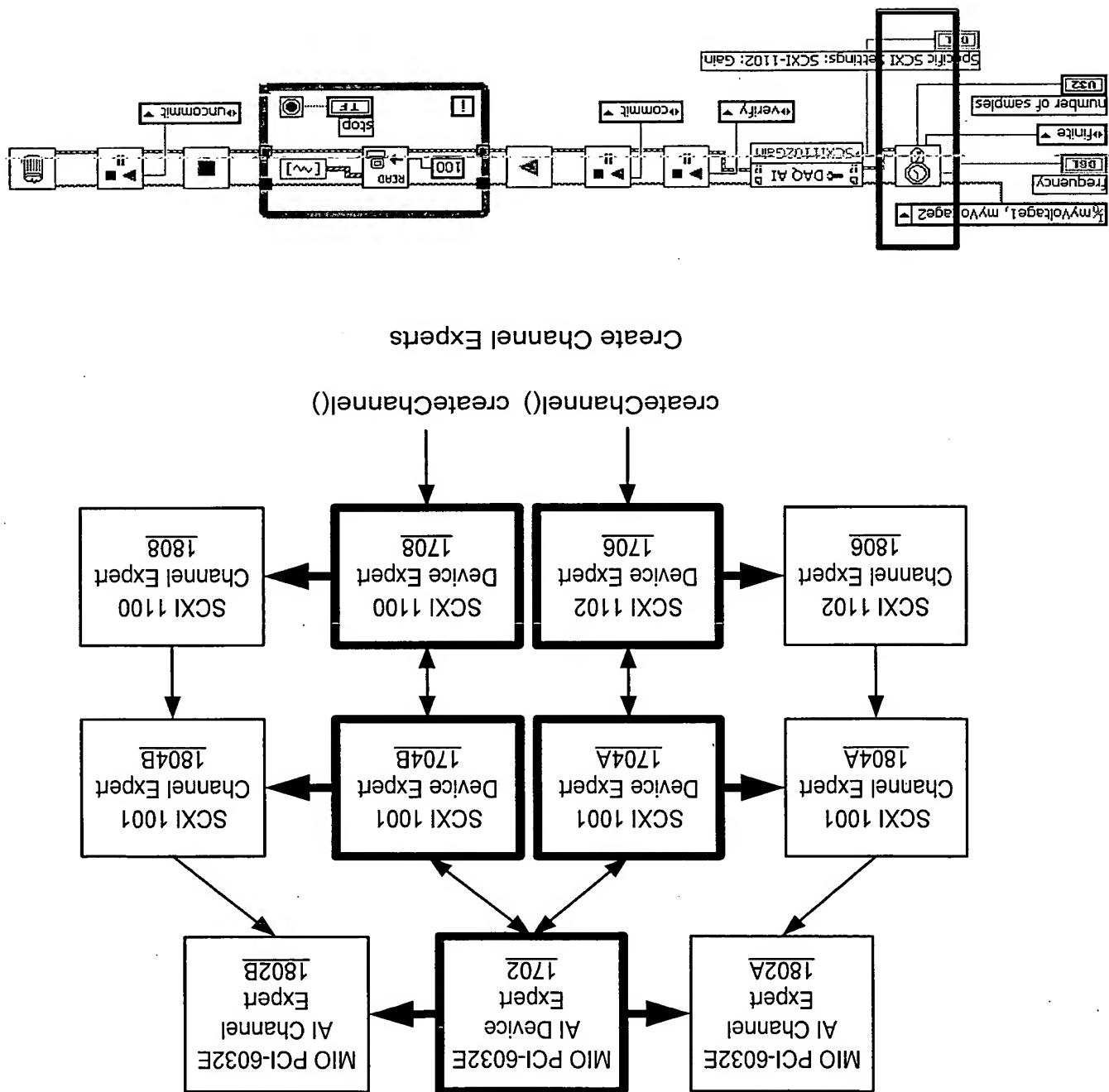


Figure 19

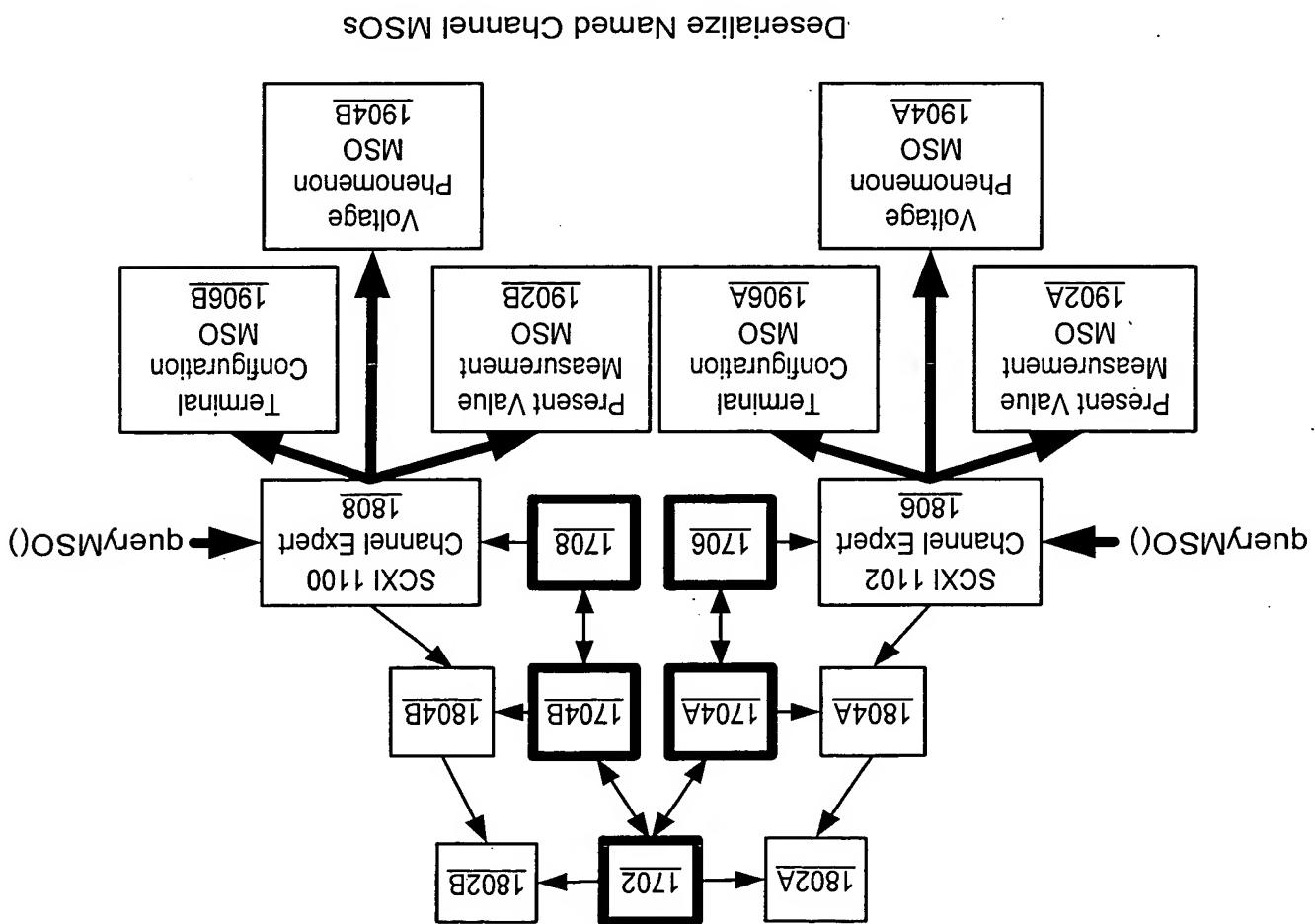
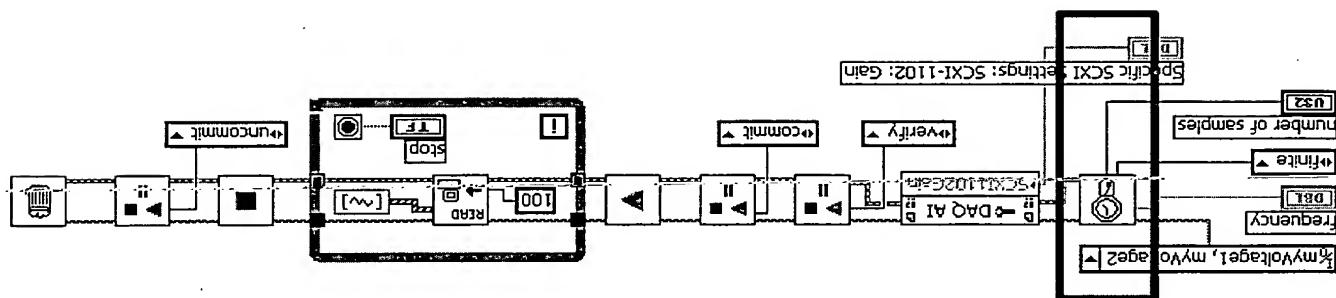


Figure 20

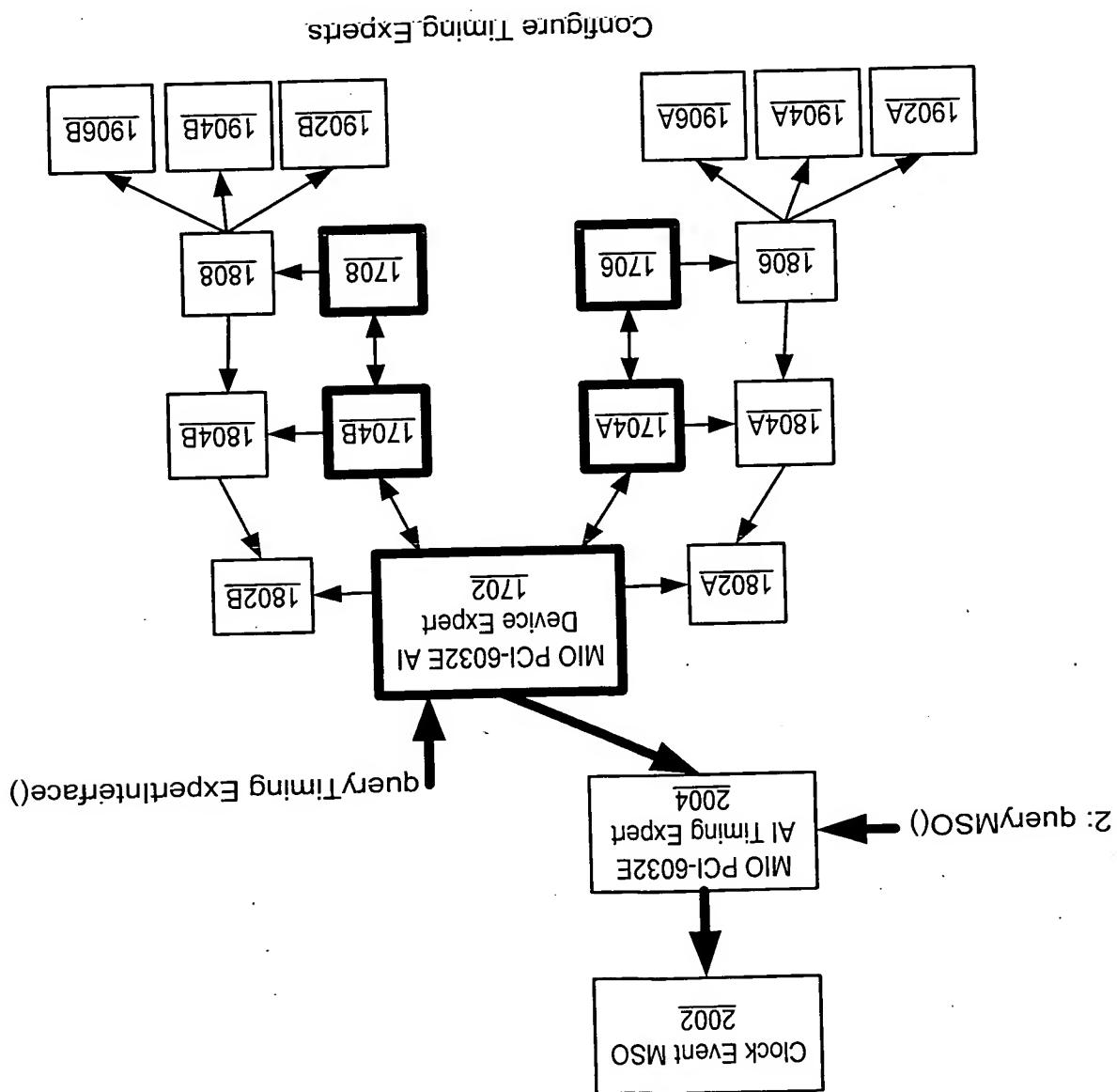
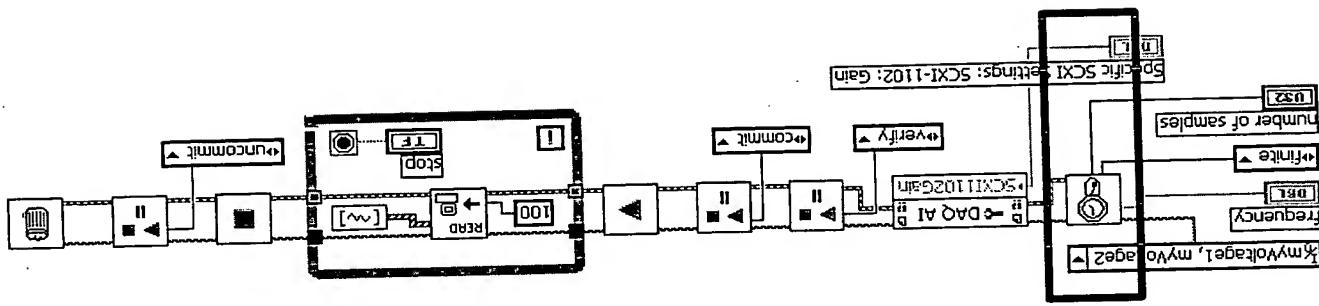
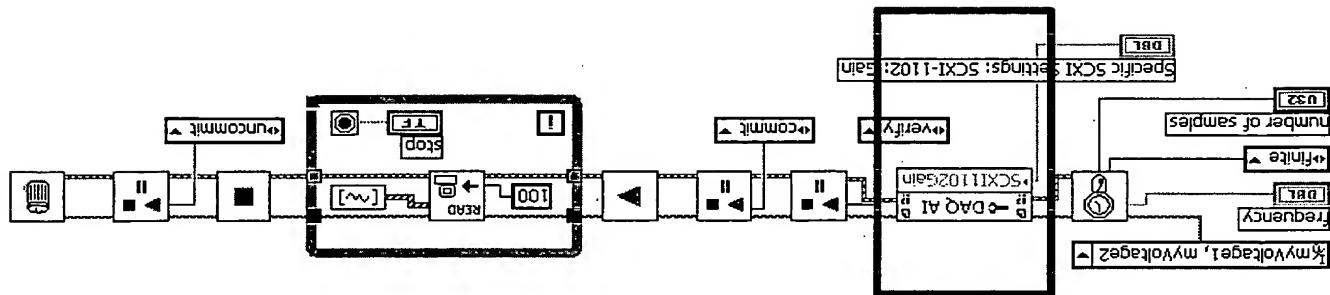


Figure 21



MSO Set Calls

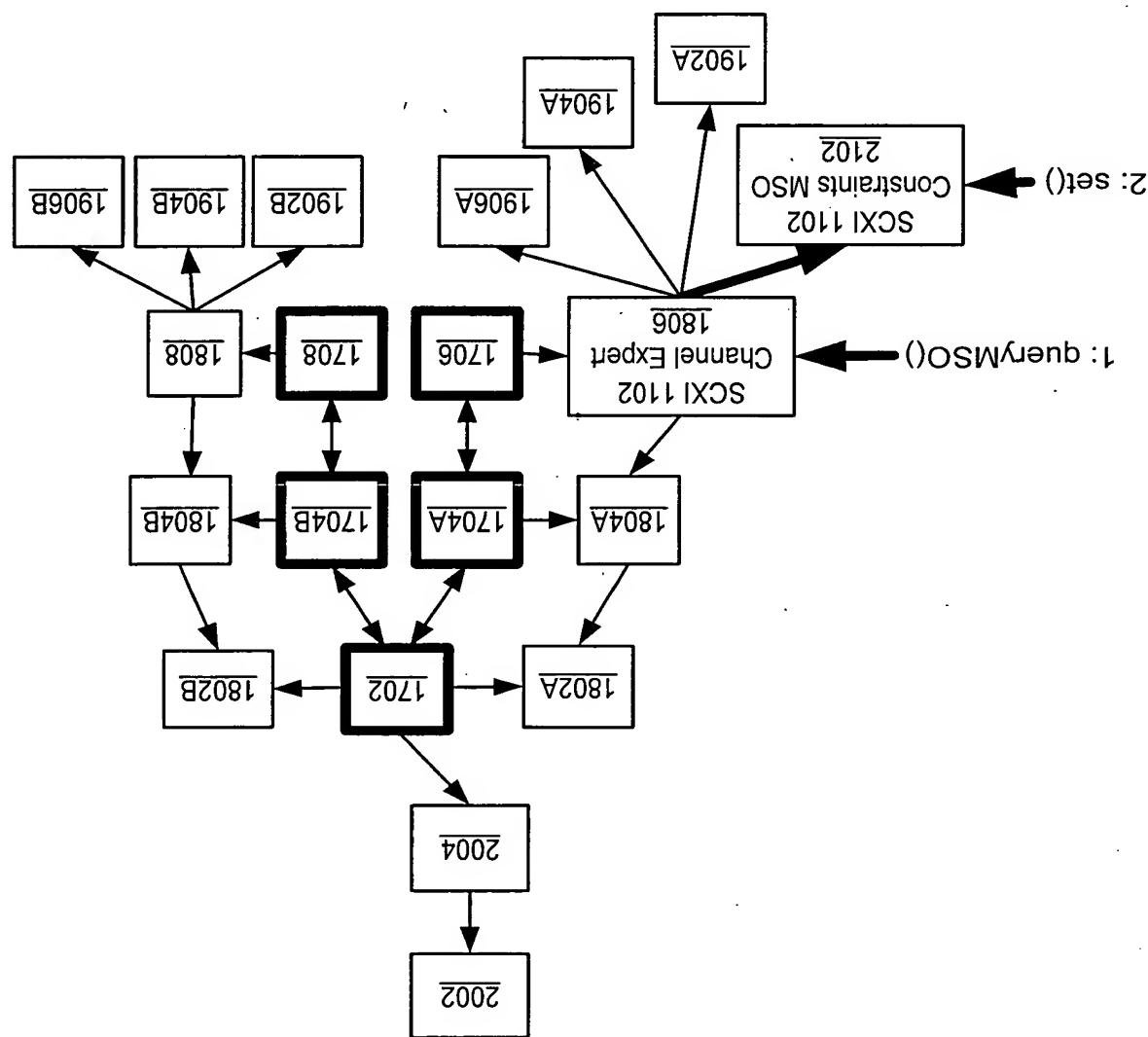
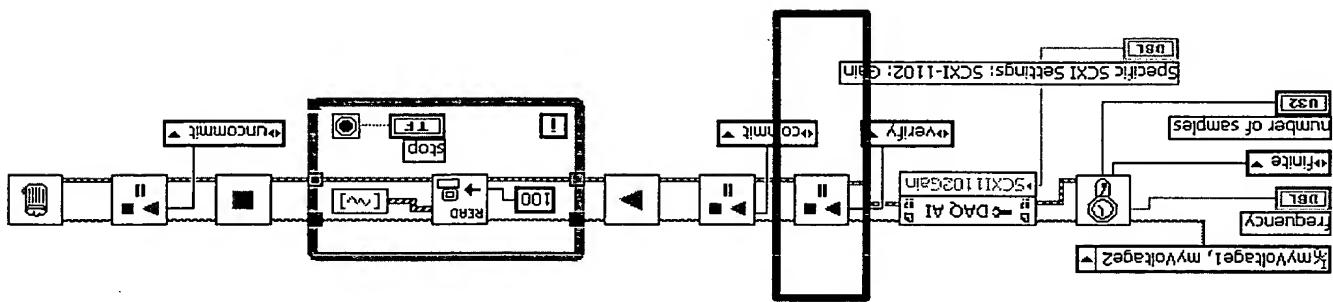


Figure 22



Analyze Channels

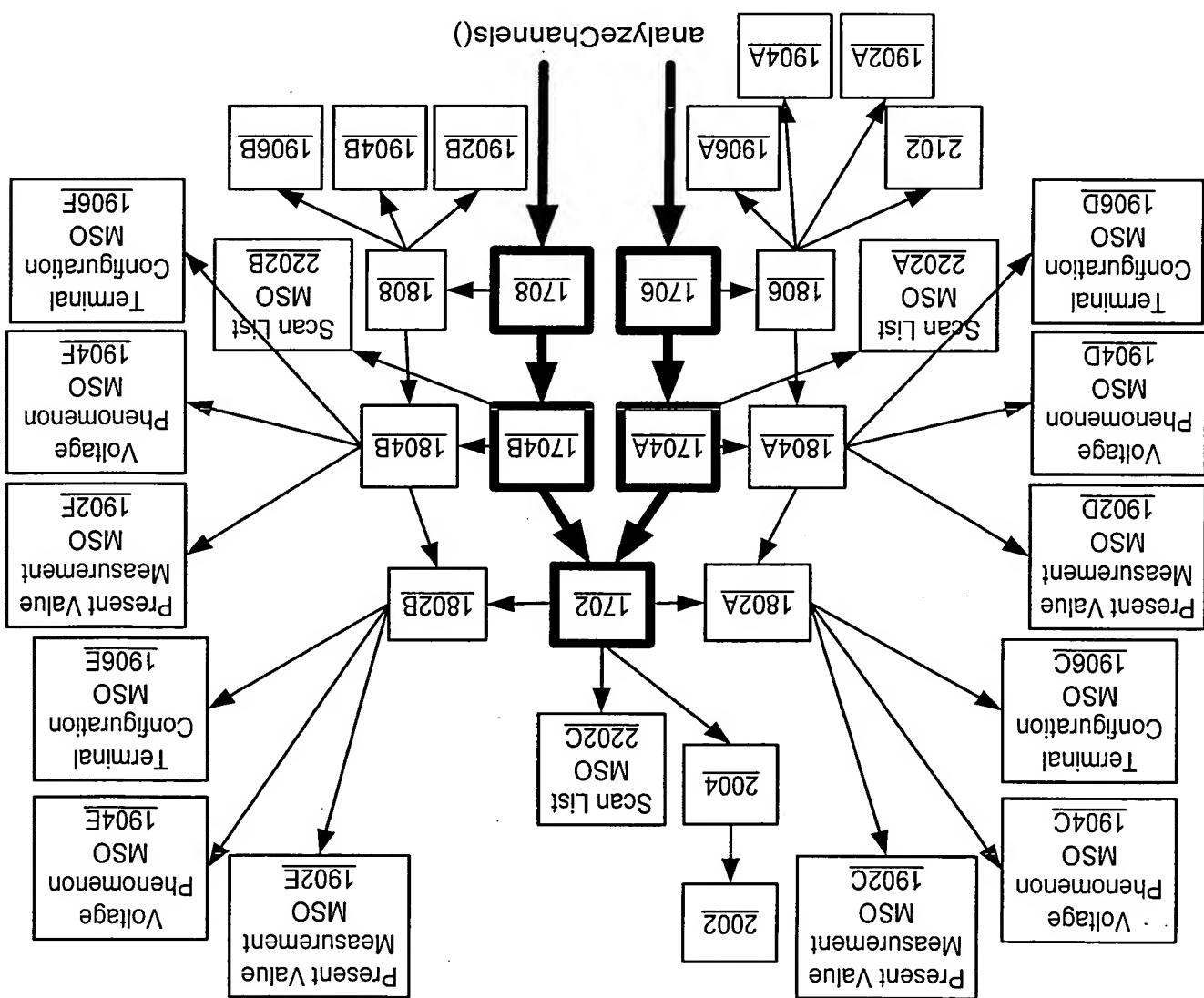
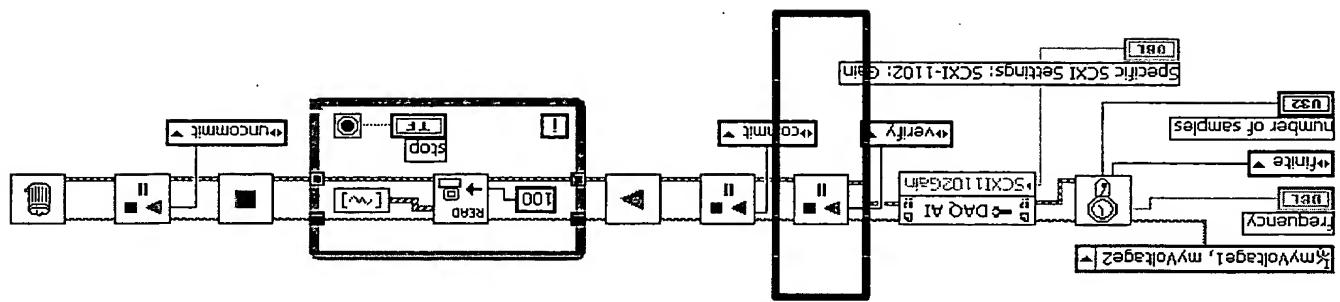


Figure 23



Analyze Timing

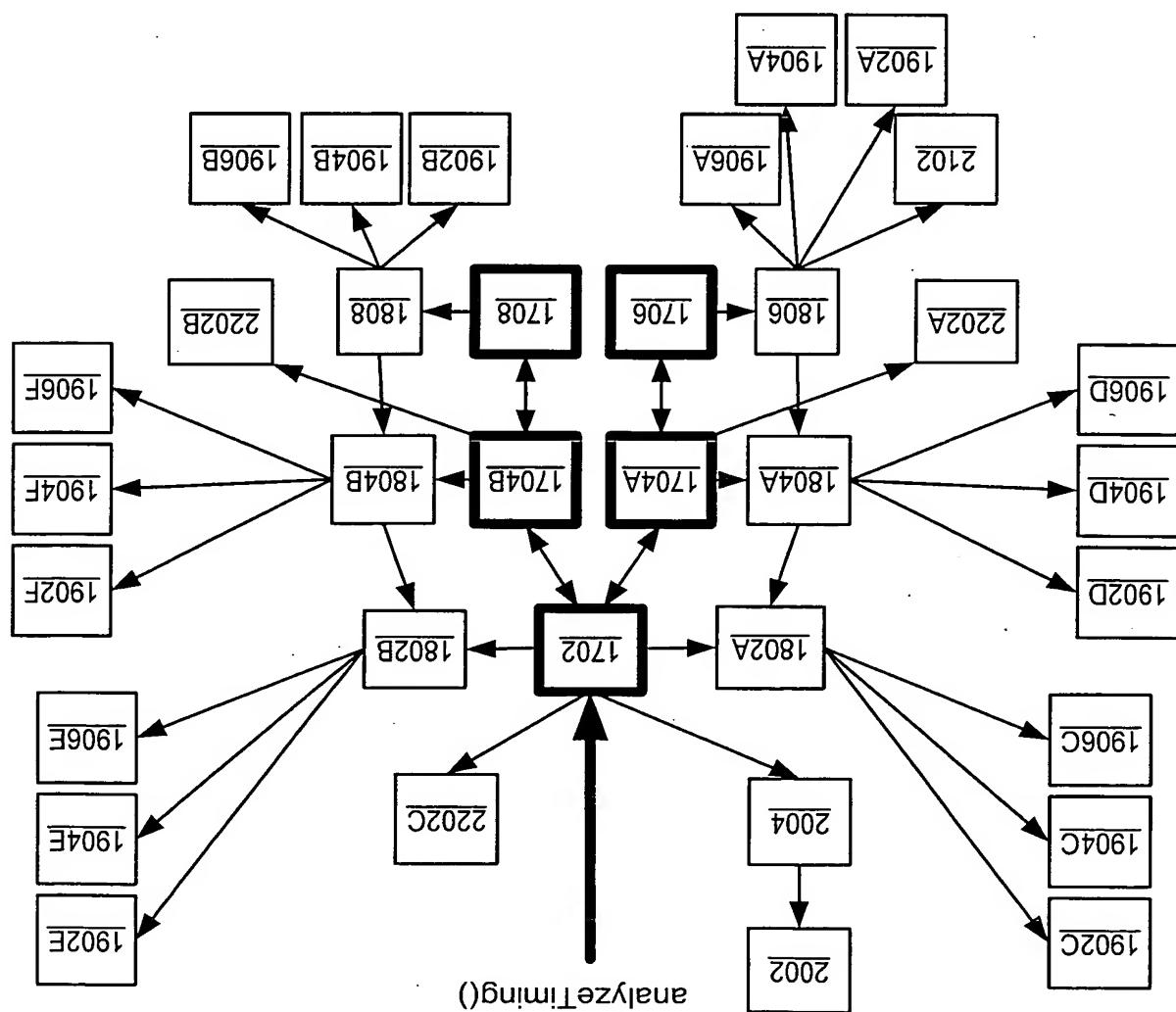
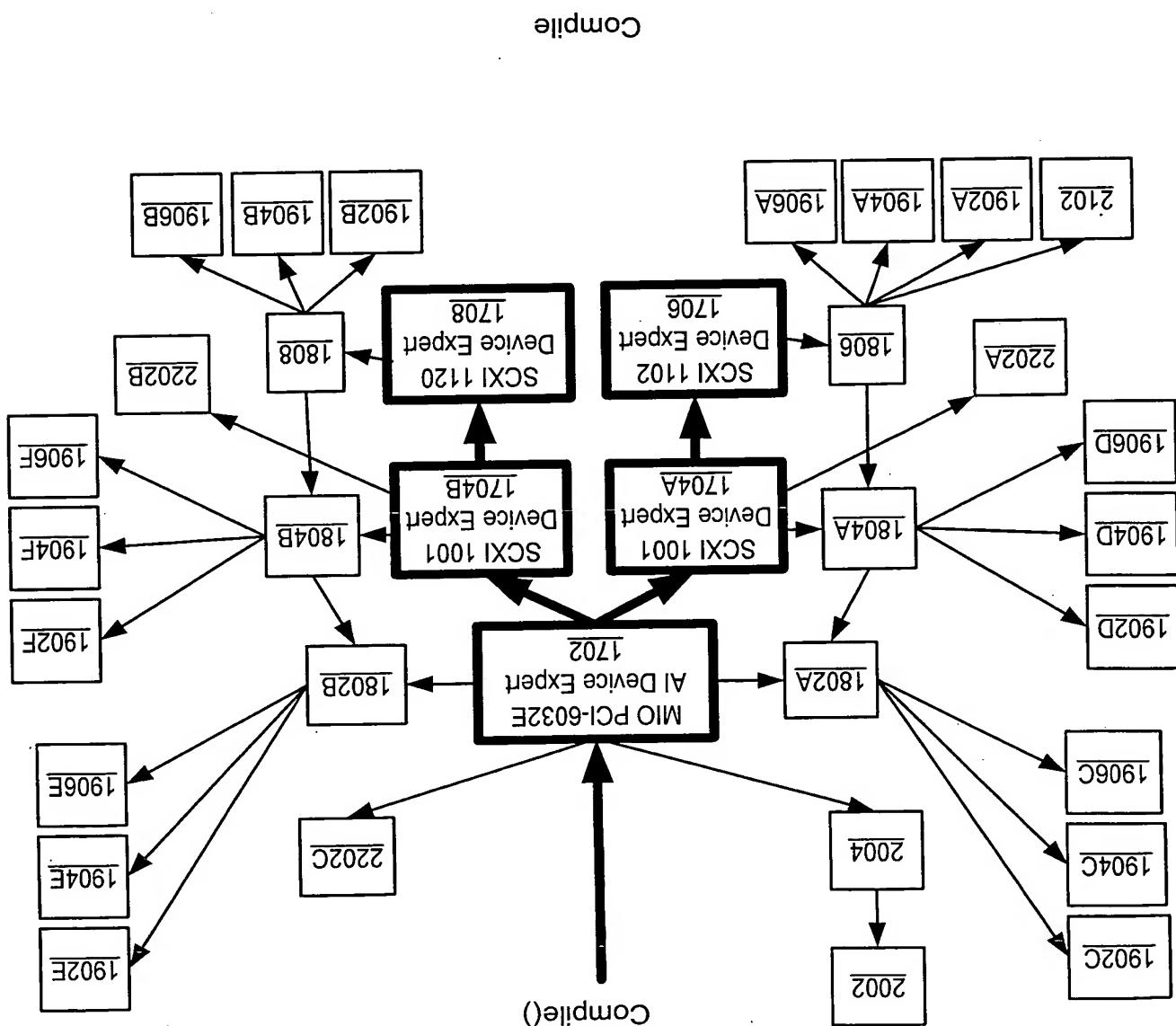
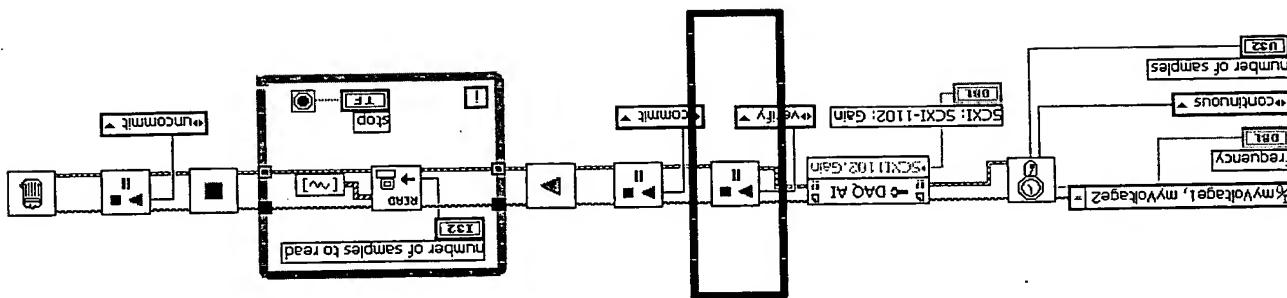


Figure 24A



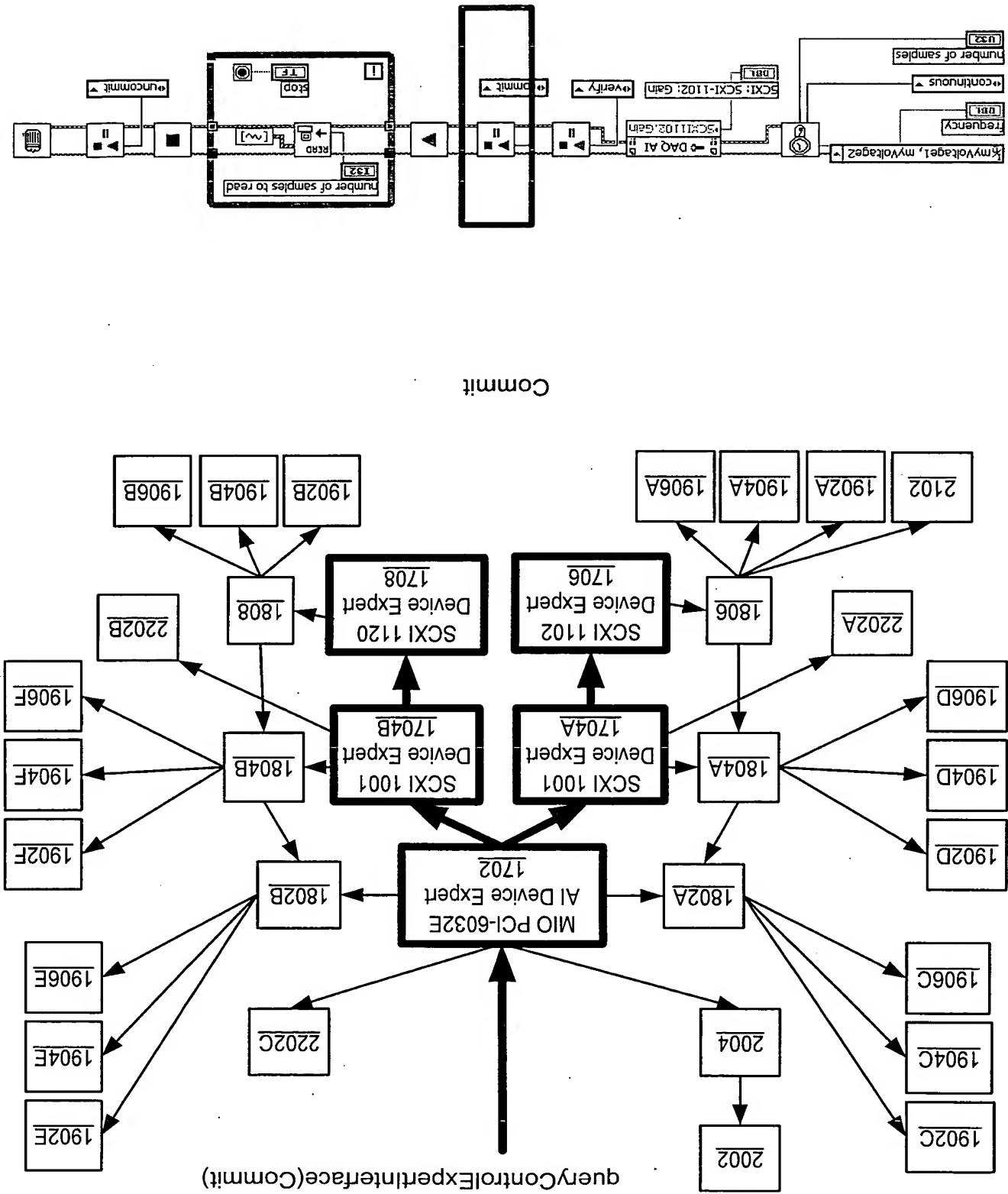


Figure 24C

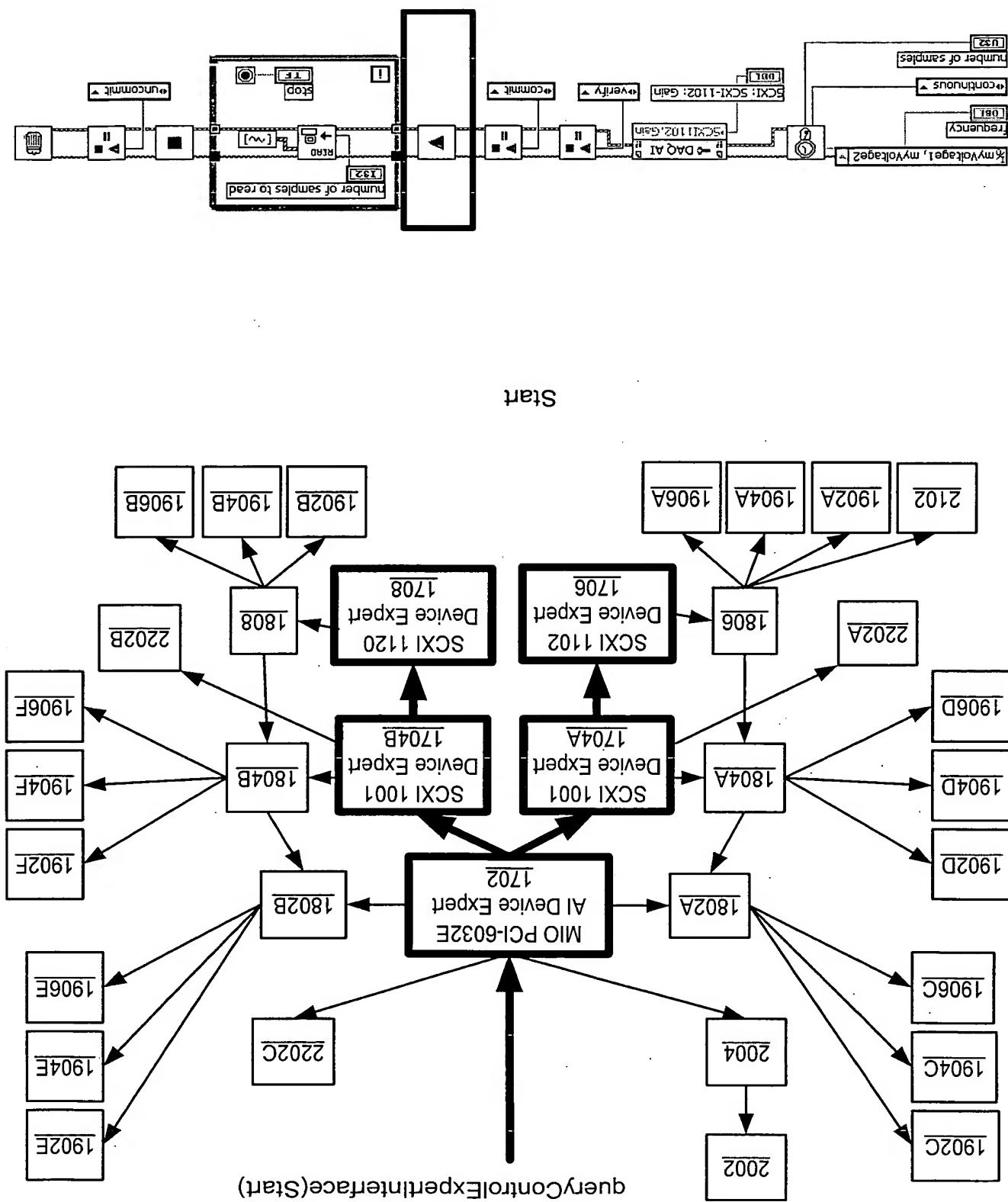


Figure 24D

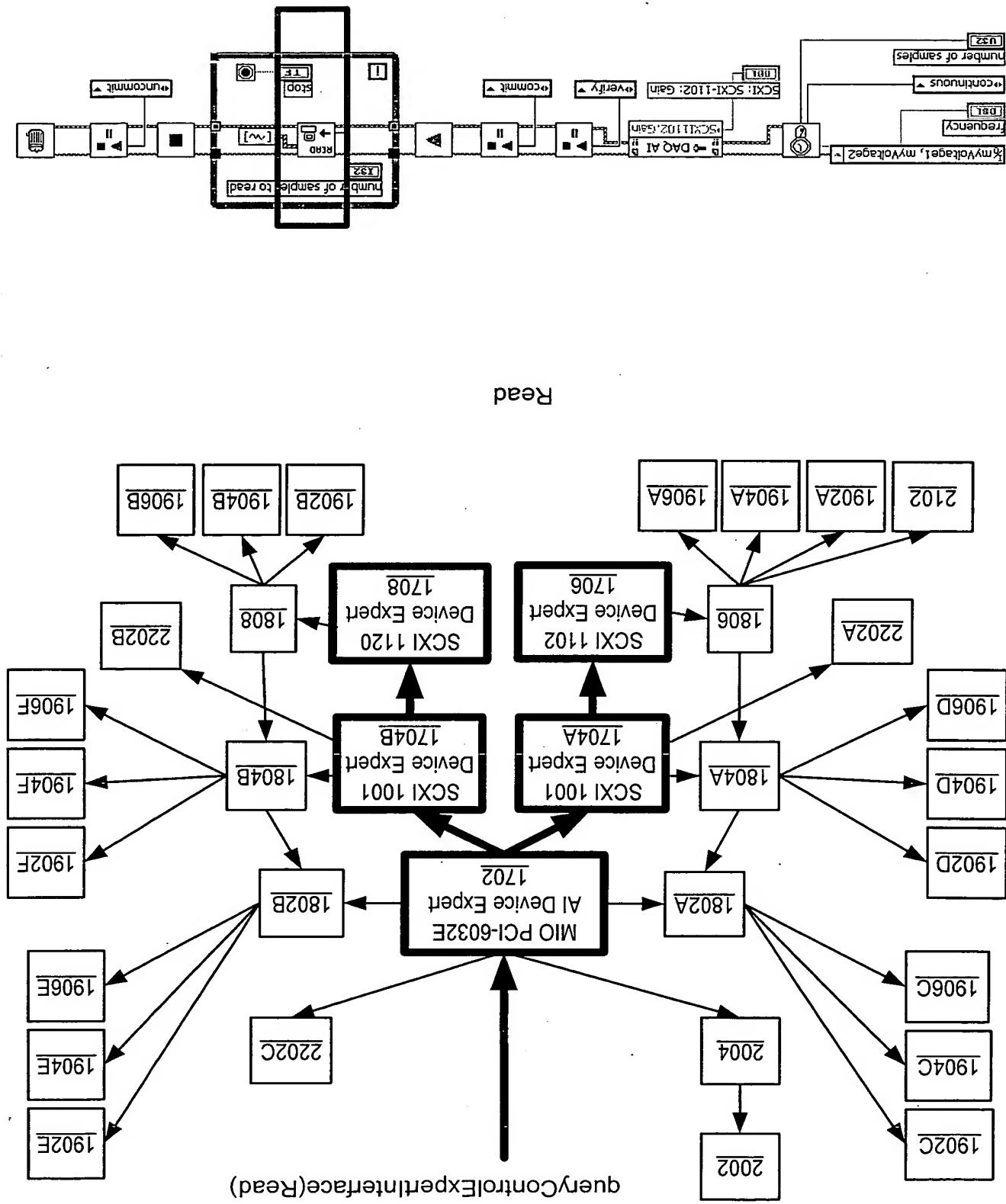


Figure 24E

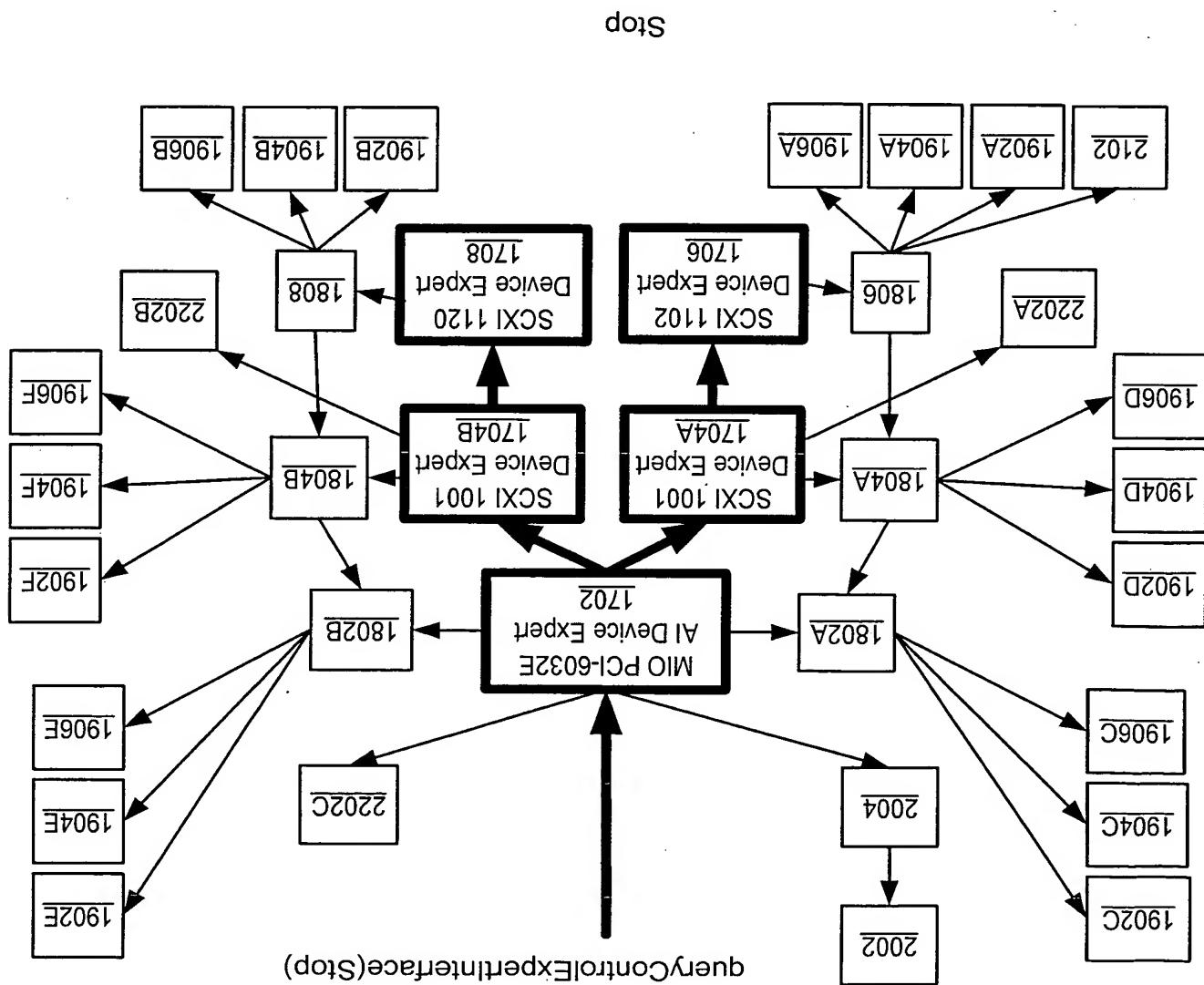
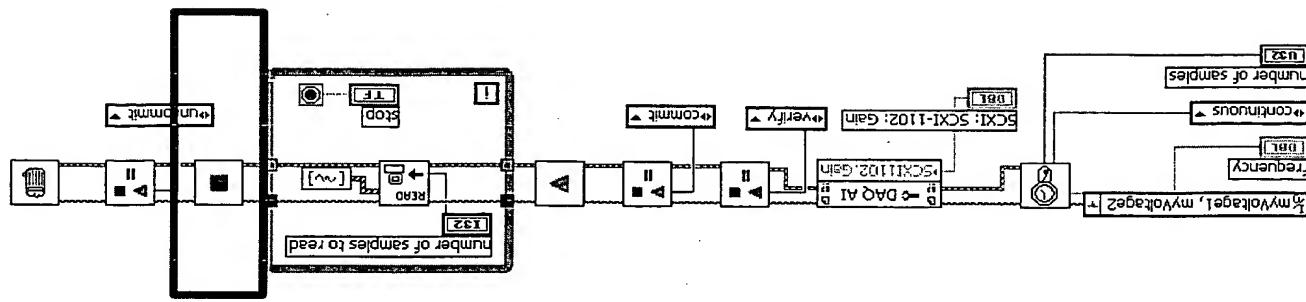
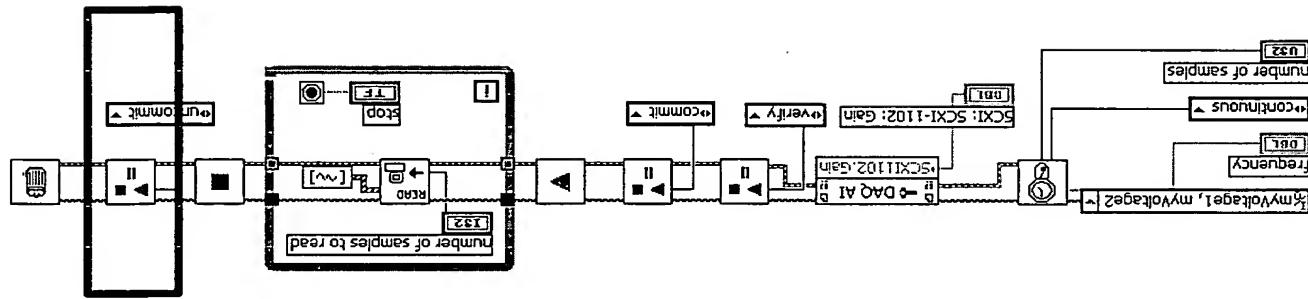
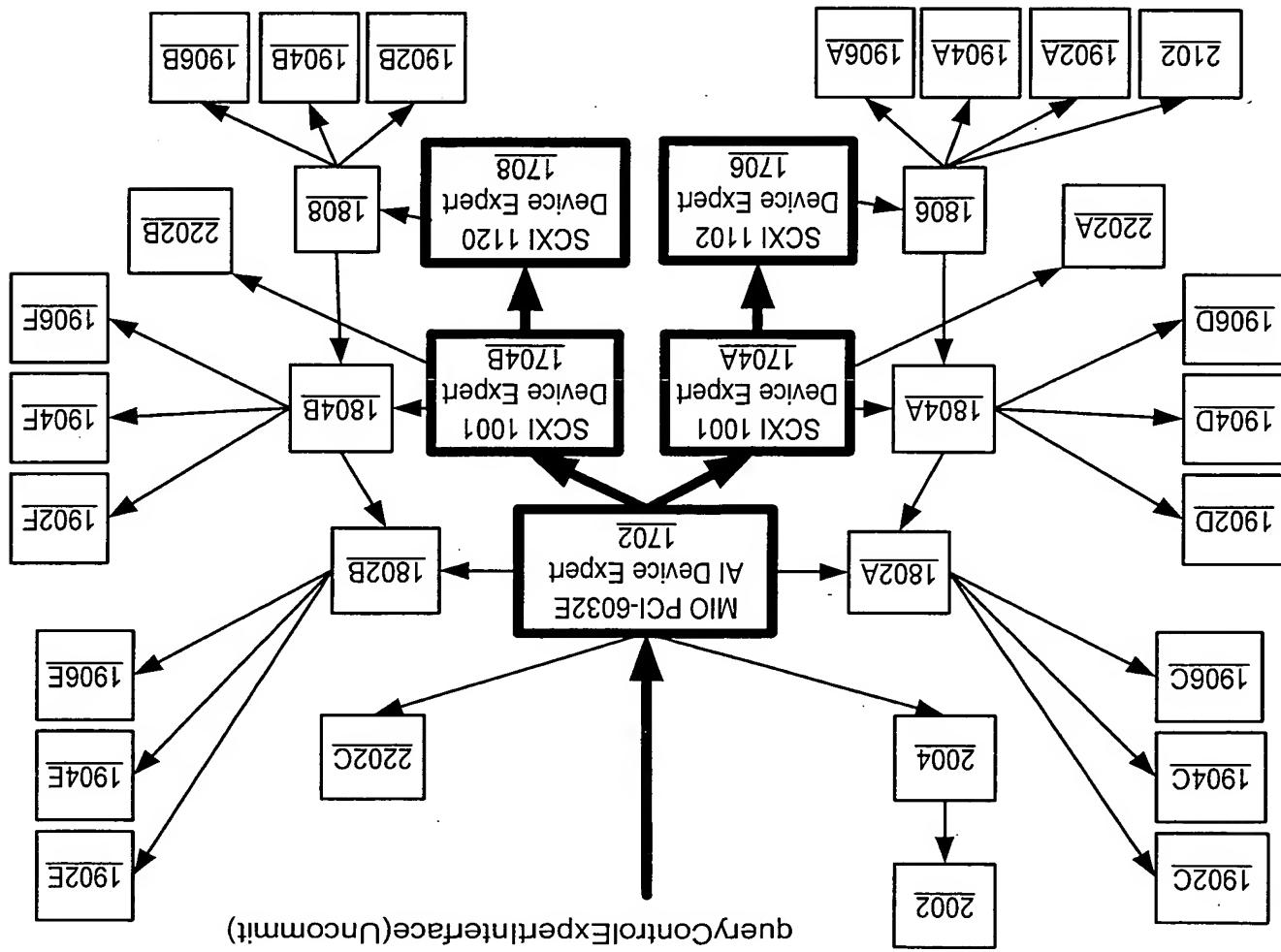


Figure 24F



Uncomit



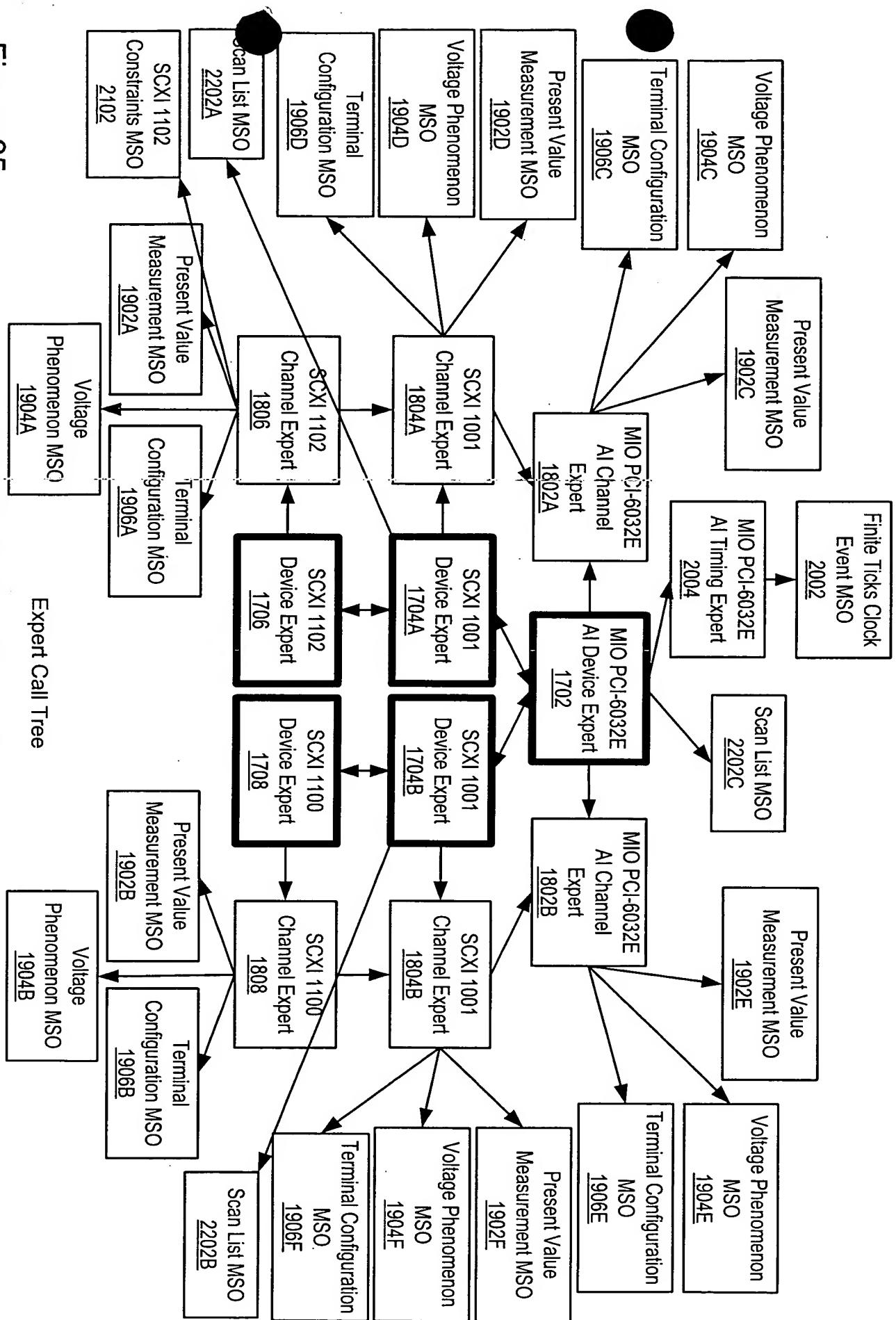
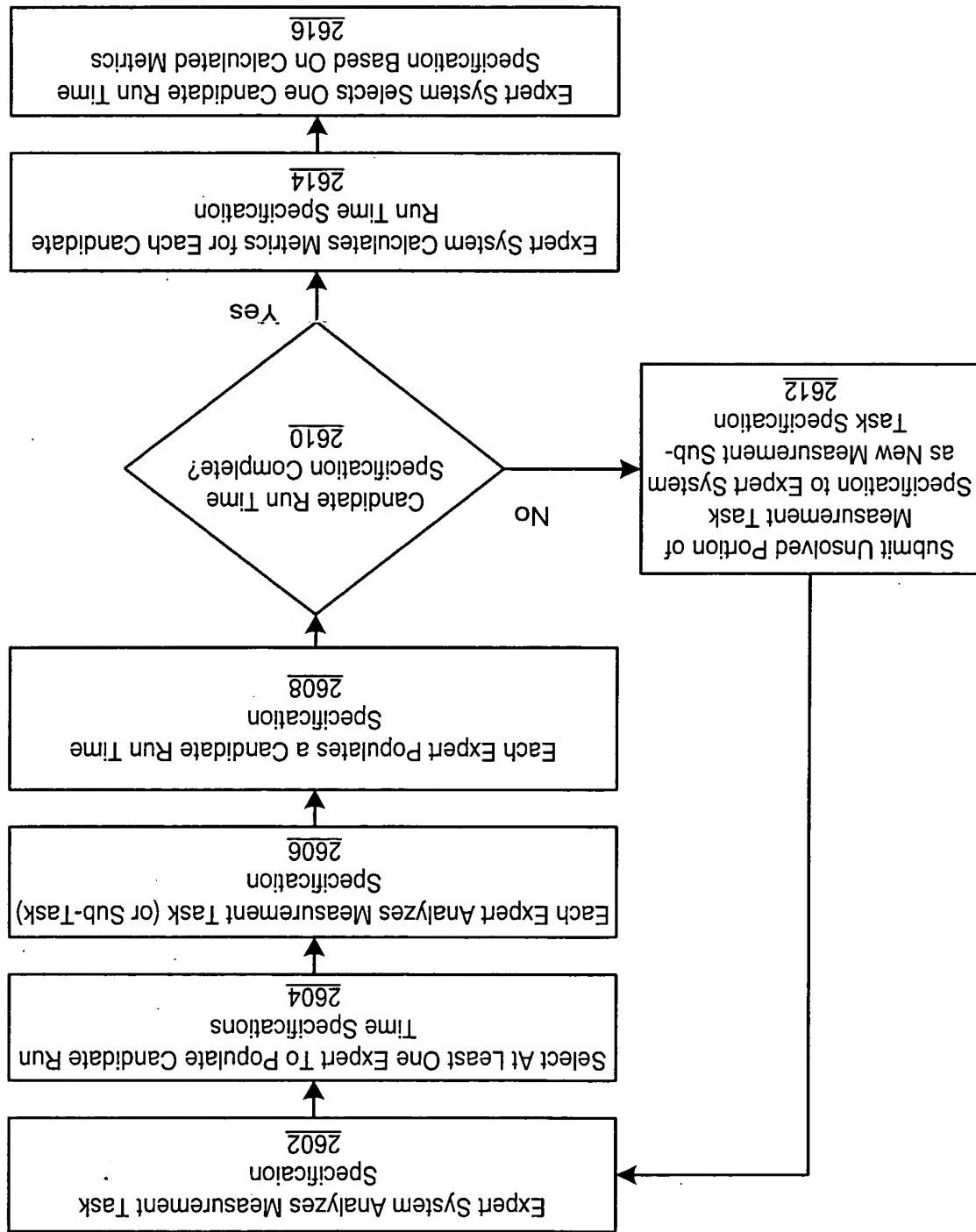


Figure 25

Figure 26



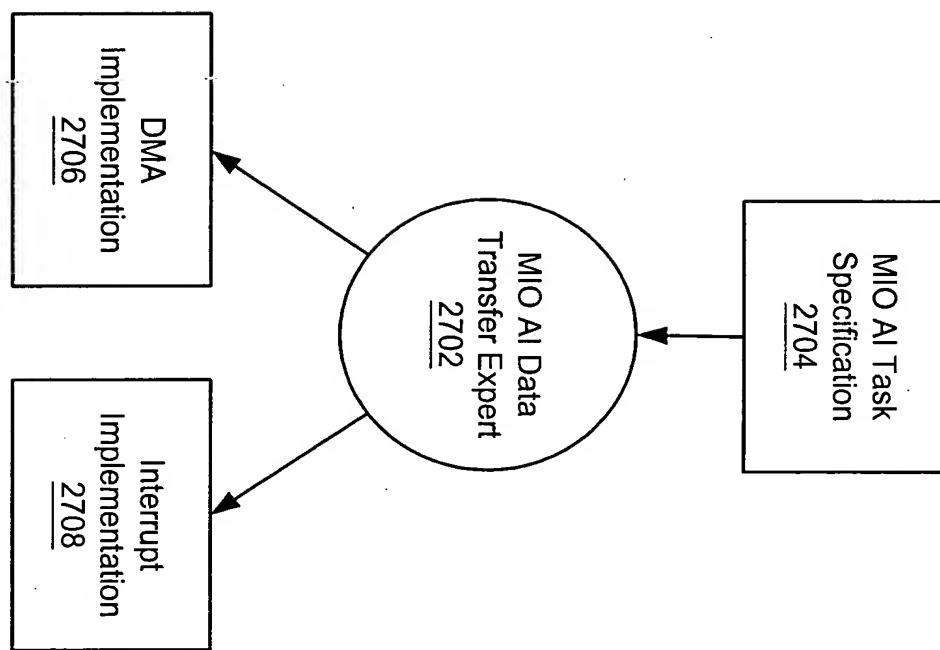


Figure 27

Figure 28

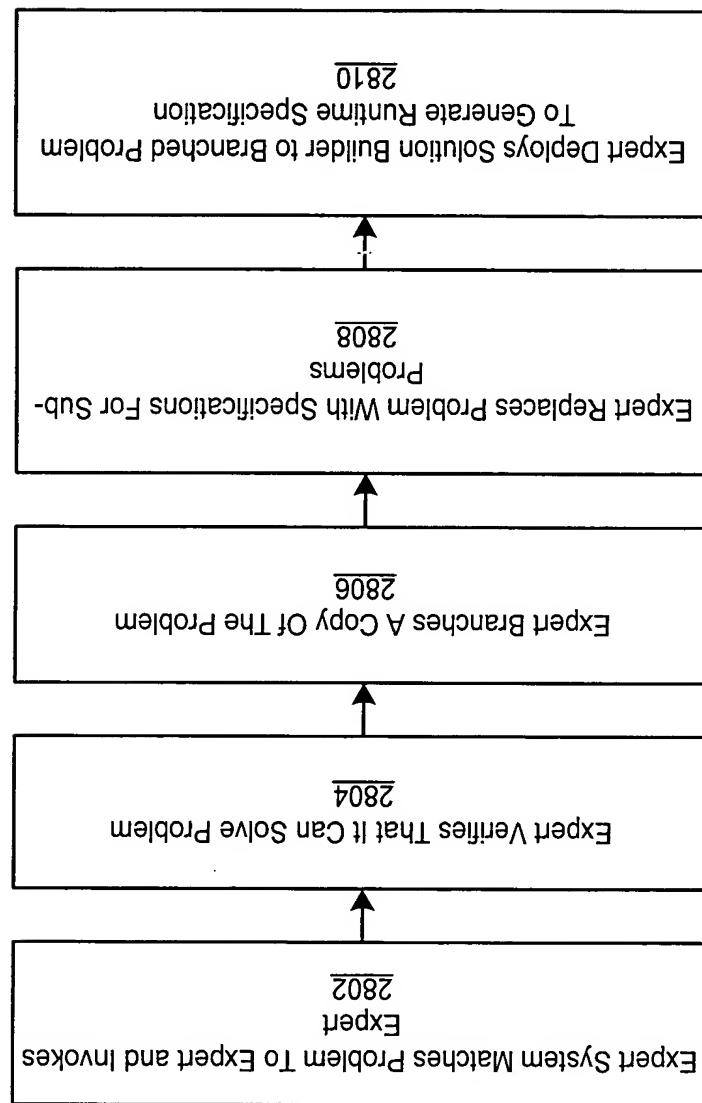
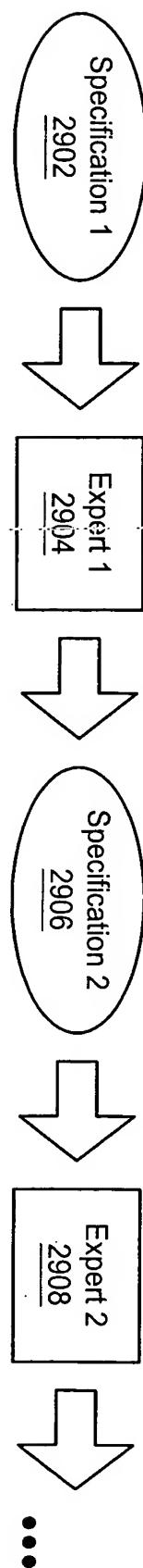


Figure 29



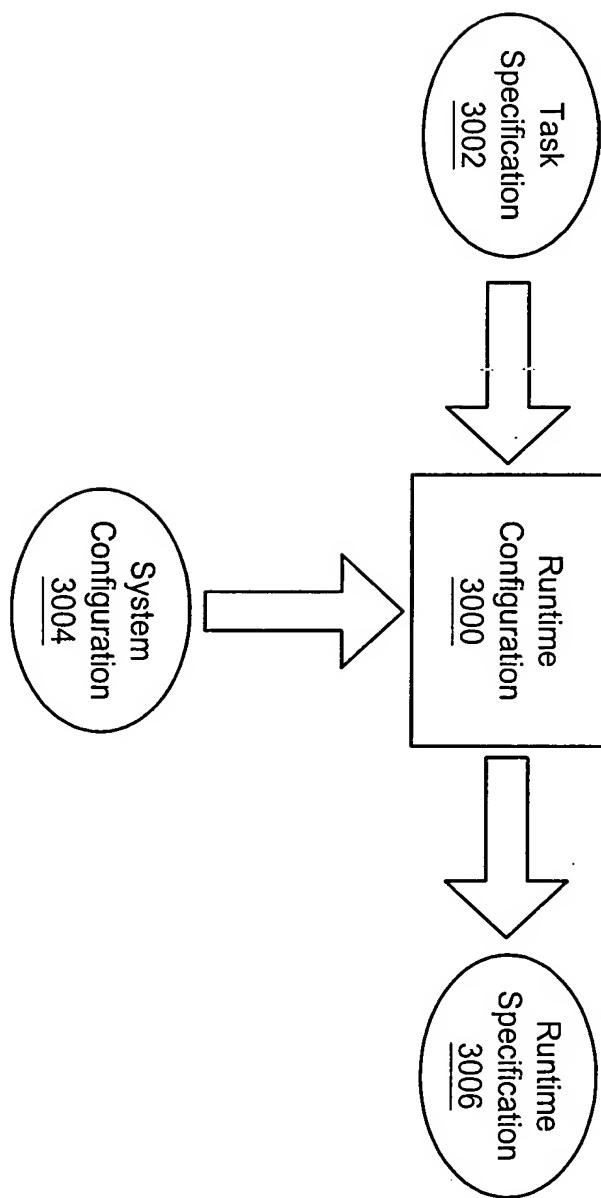


Figure 30

Figure 31

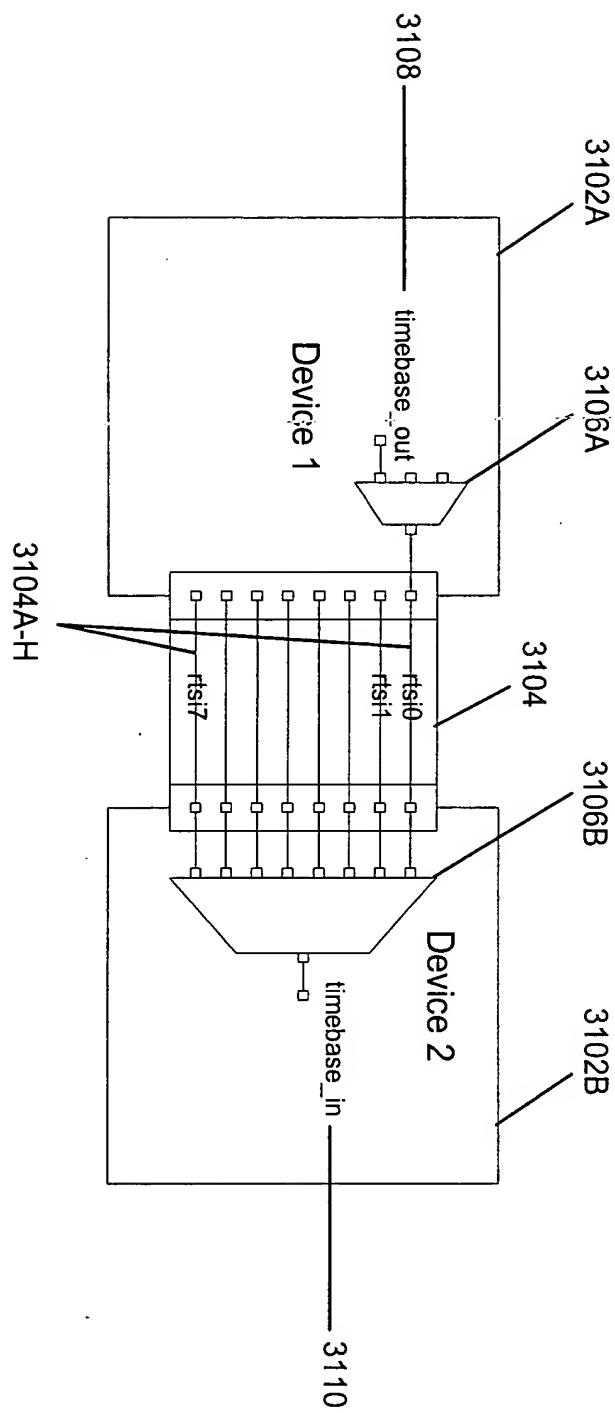
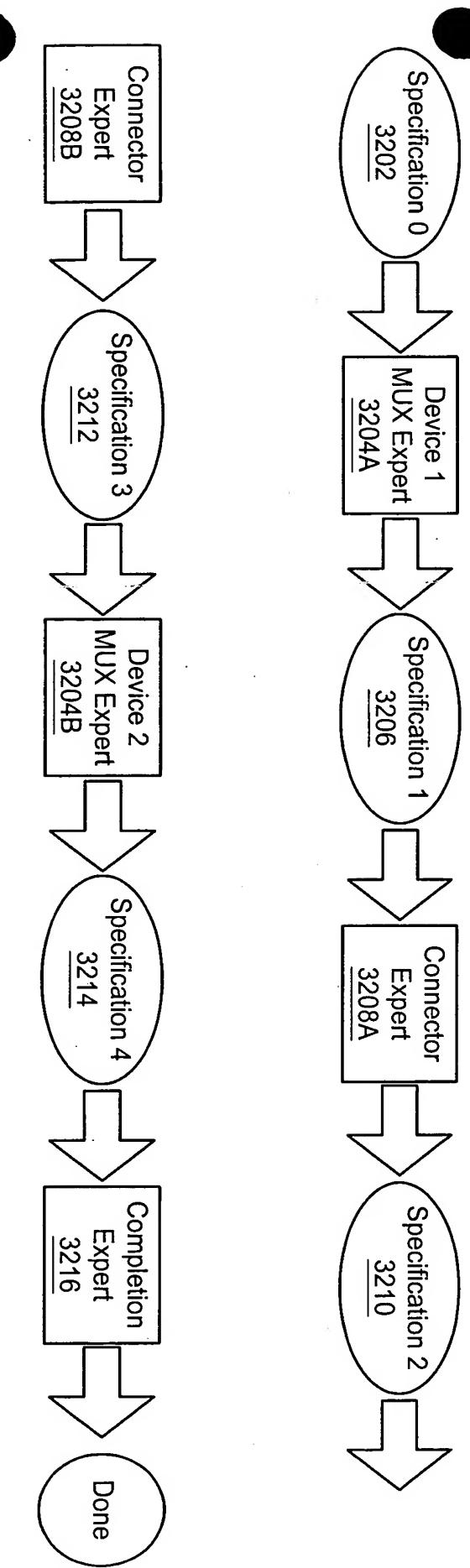


Figure 32



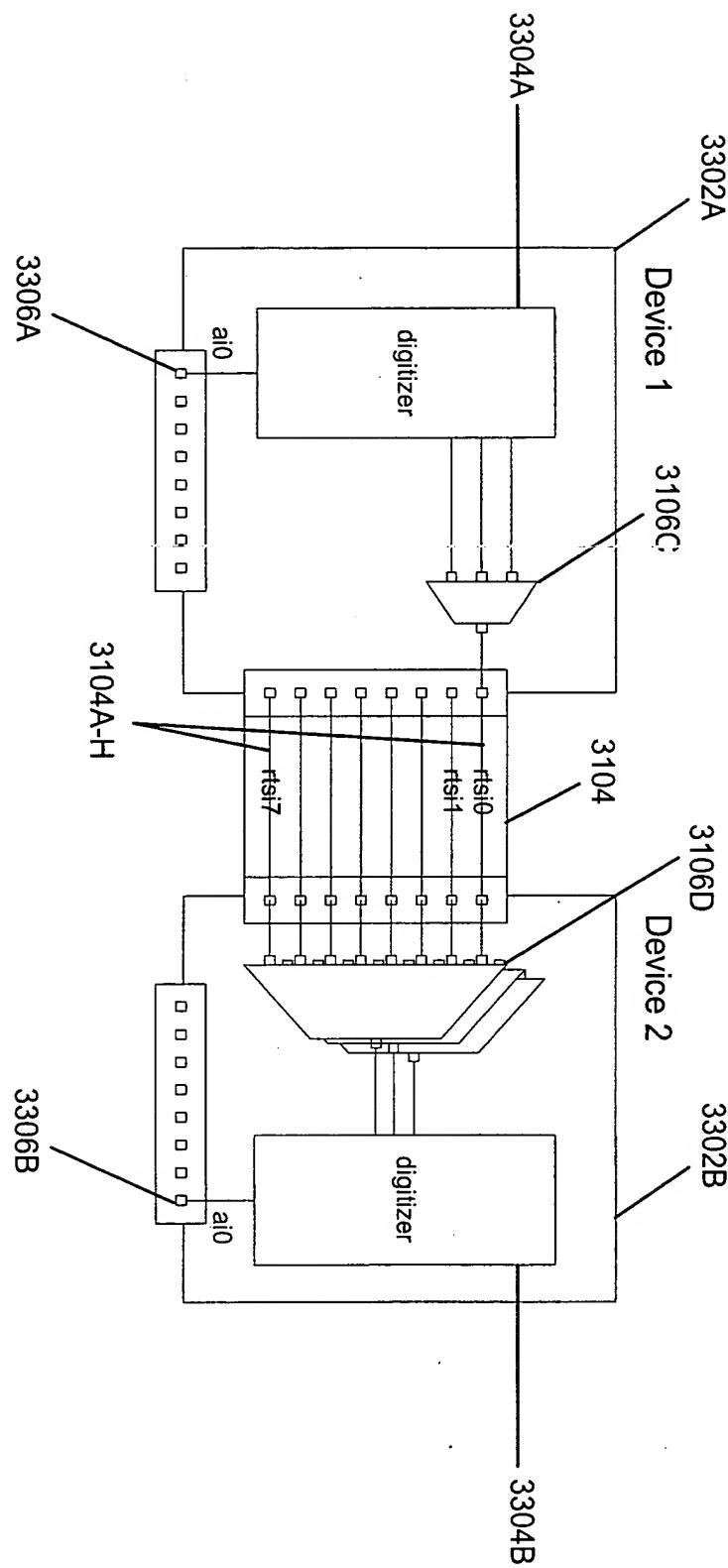


Figure 33

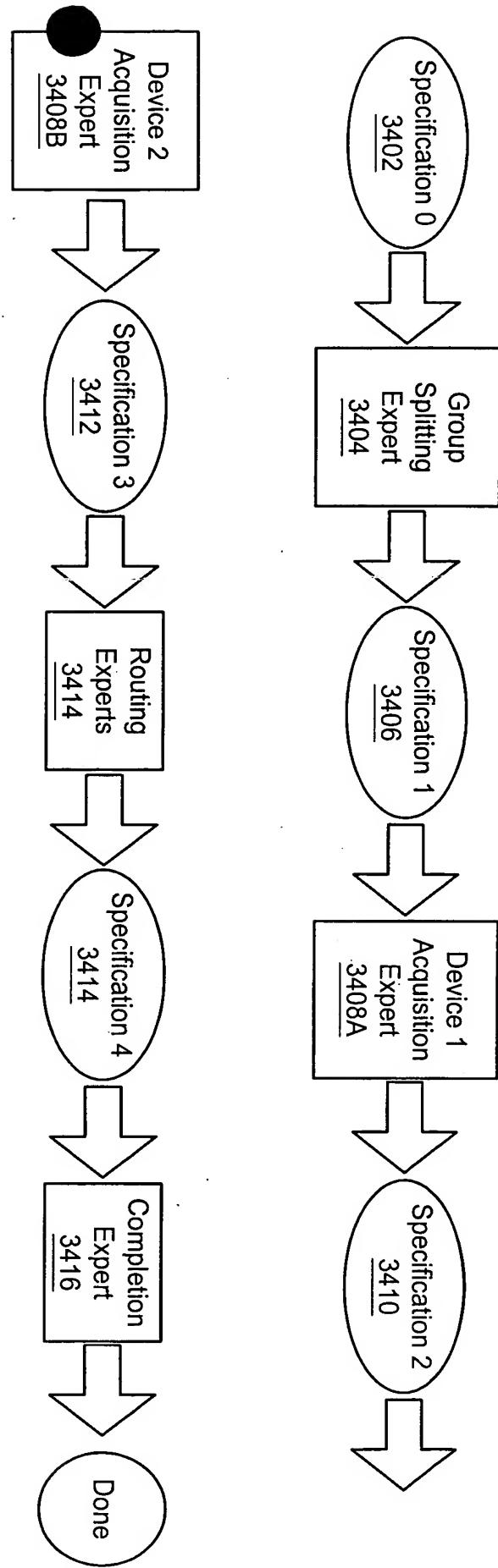


Figure 34

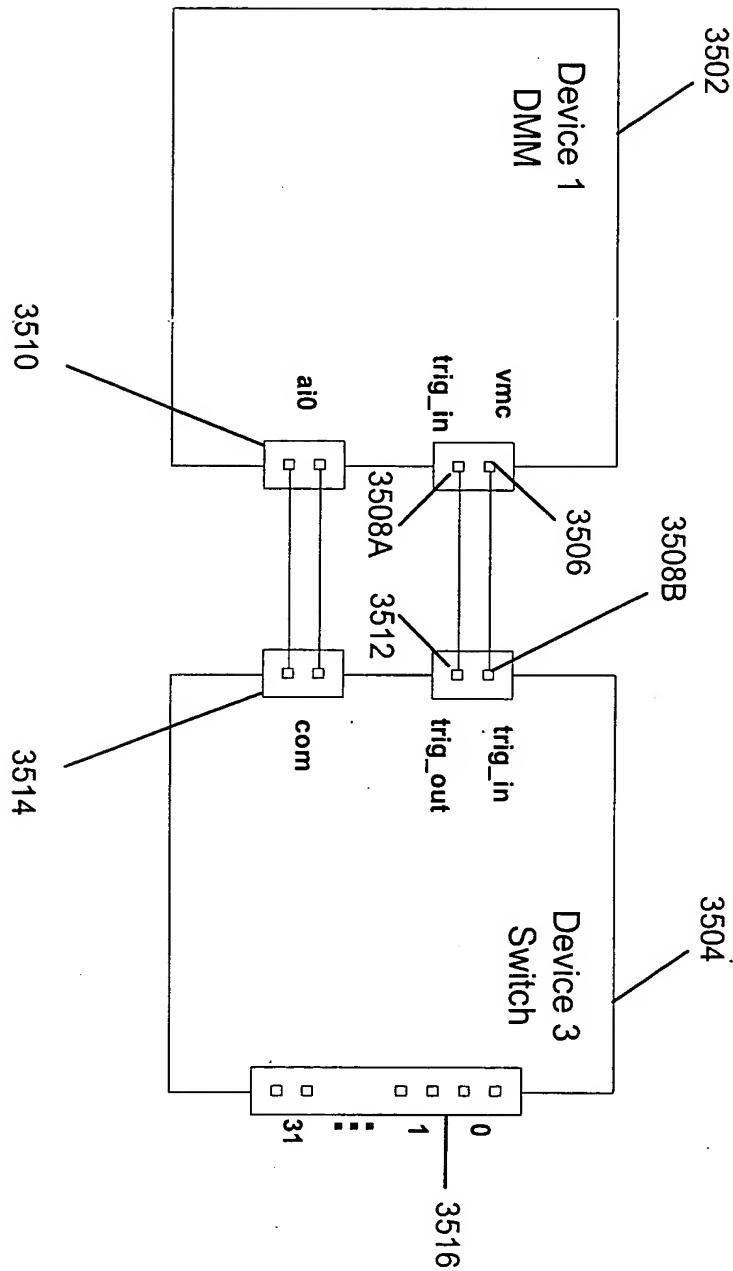


Figure 35

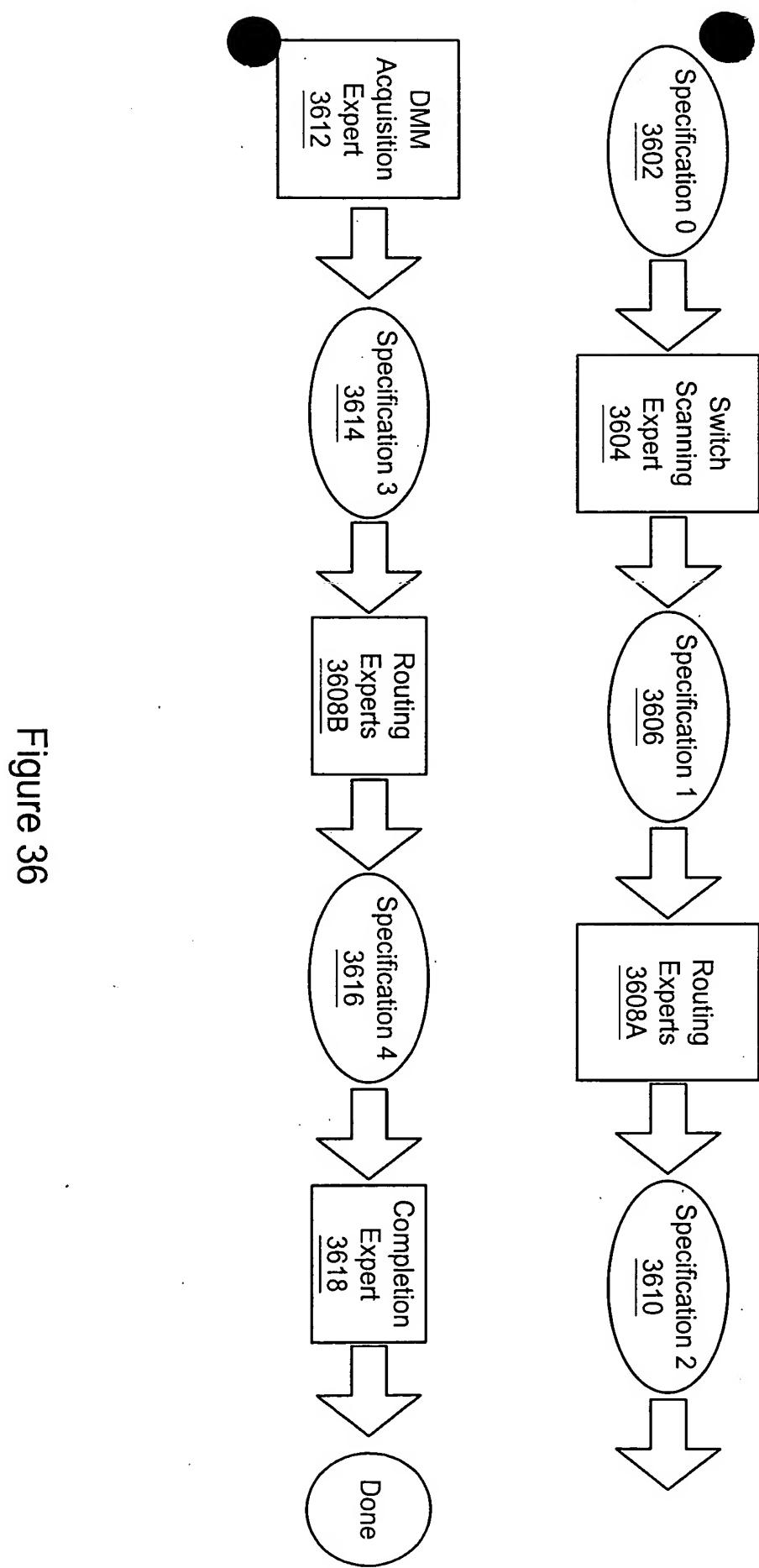


Figure 36

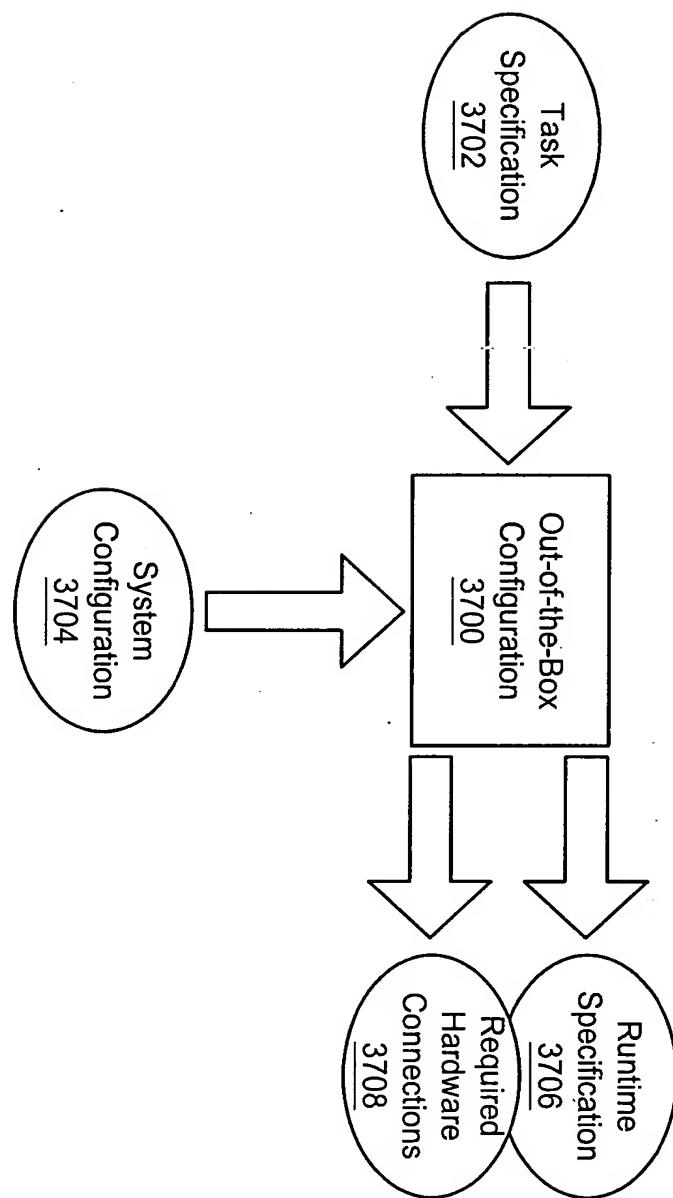
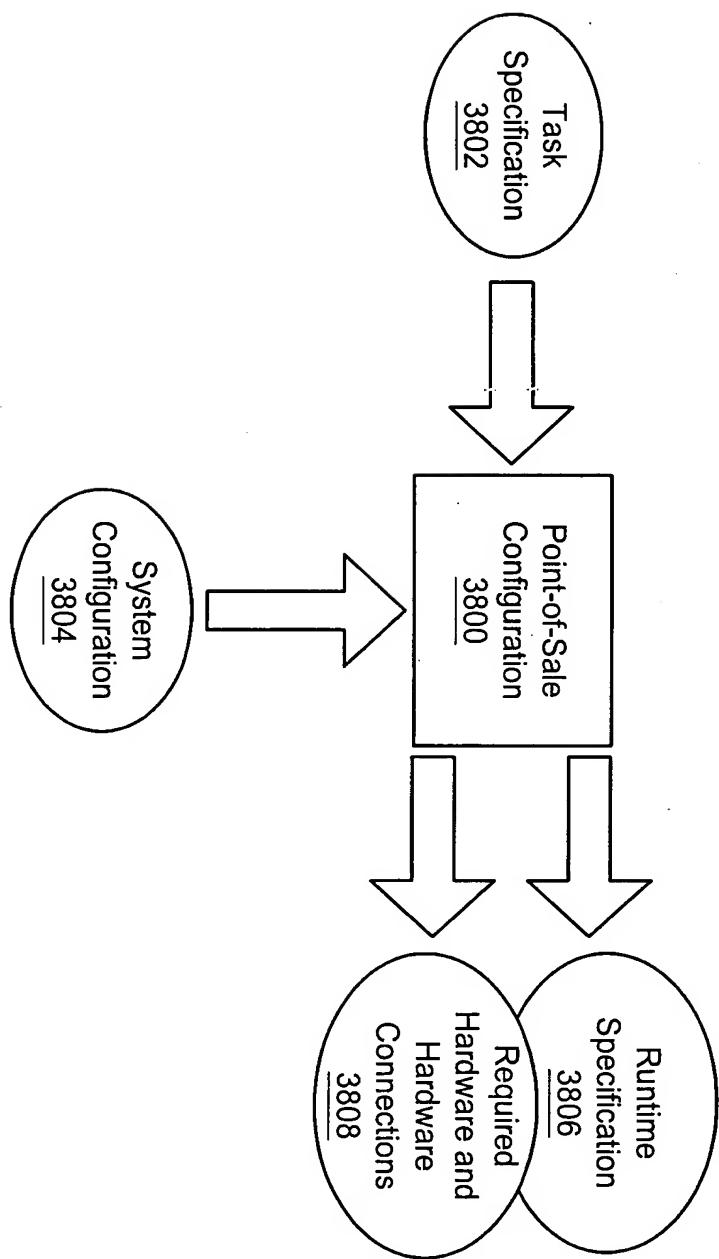
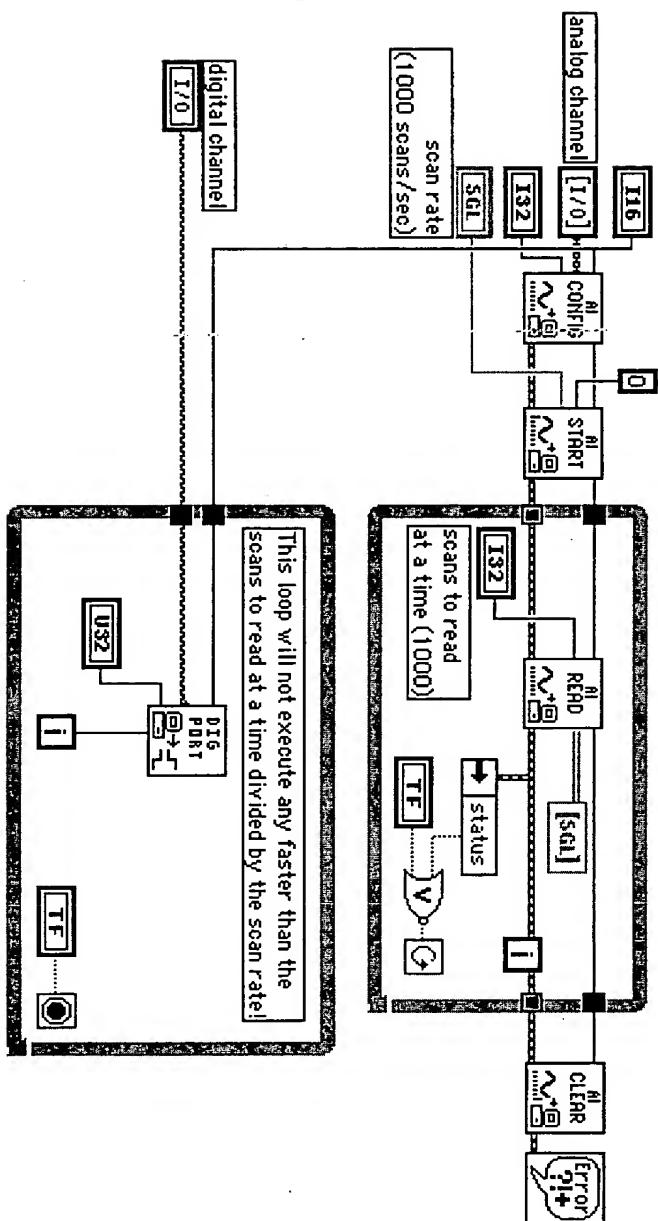


Figure 37

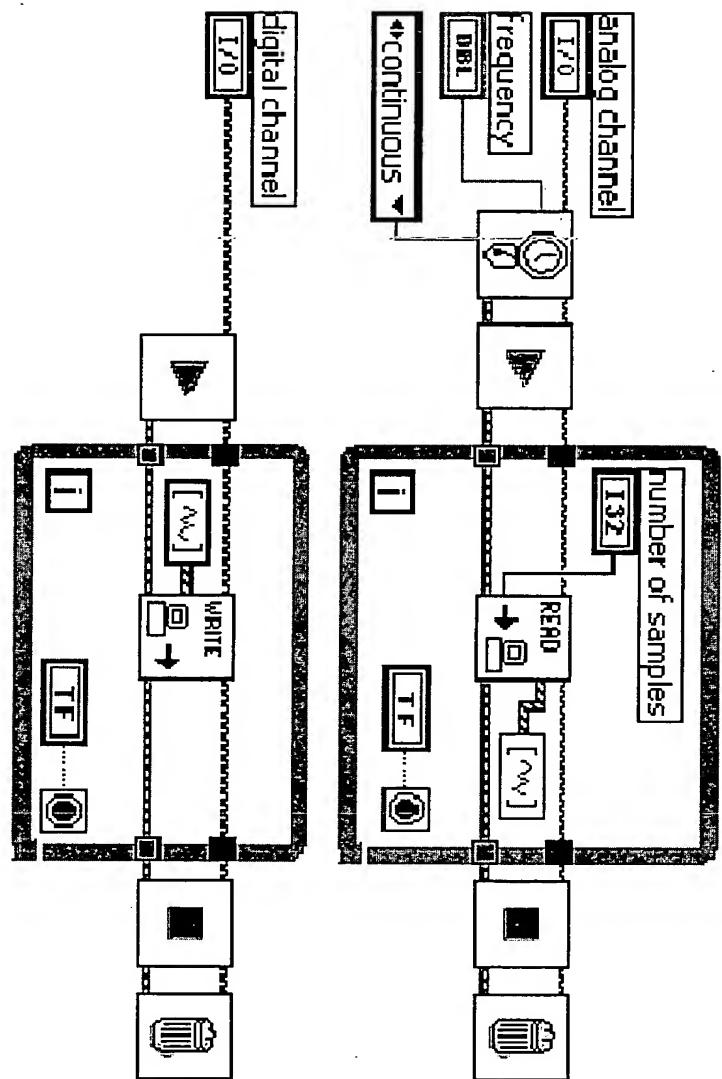
Figure 38





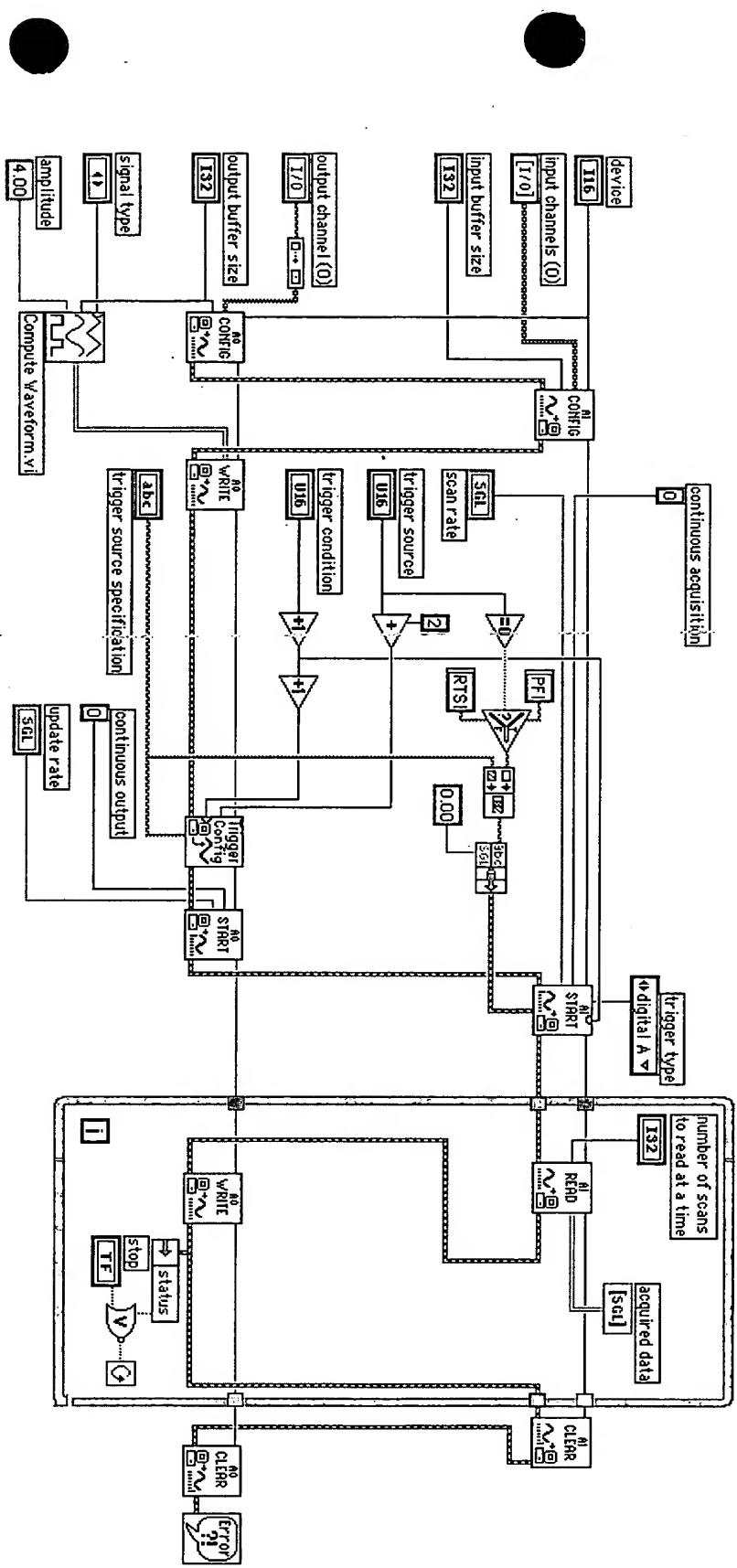
Simultaneous Buffered Analog Input And Single Point Digital Output With Single-Threaded Driver (Prior Art)

Figure 39A (Prior Art)



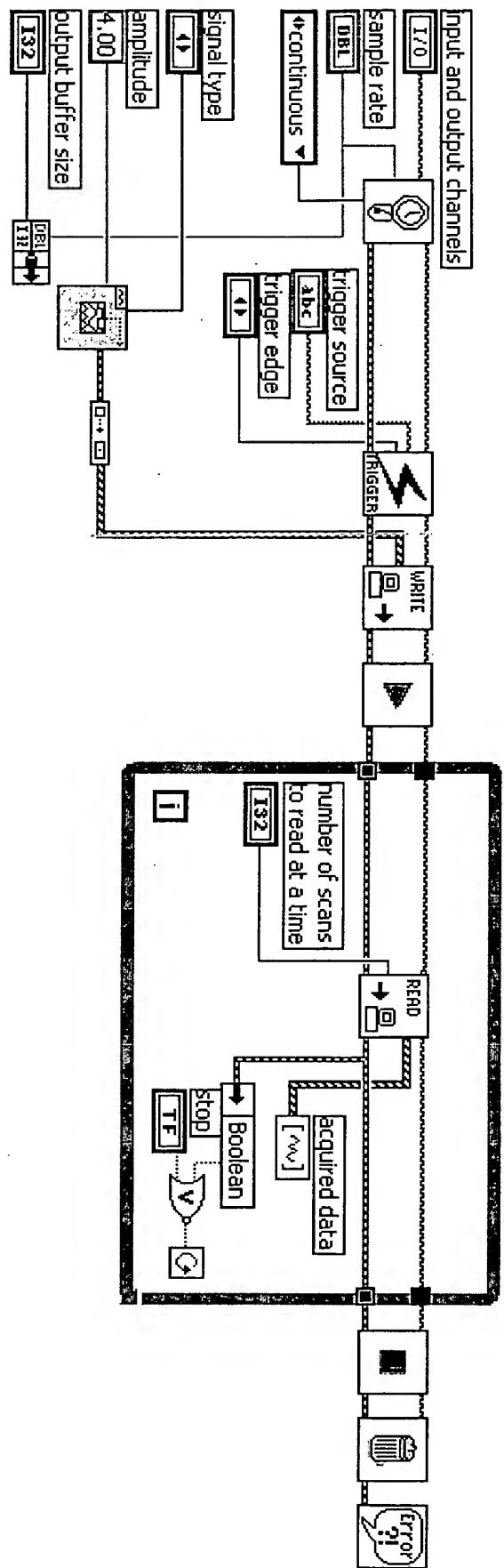
Simultaneous Buffered Analog Input And Single Point Digital Output With Multi-Threaded Driver

Figure 39B



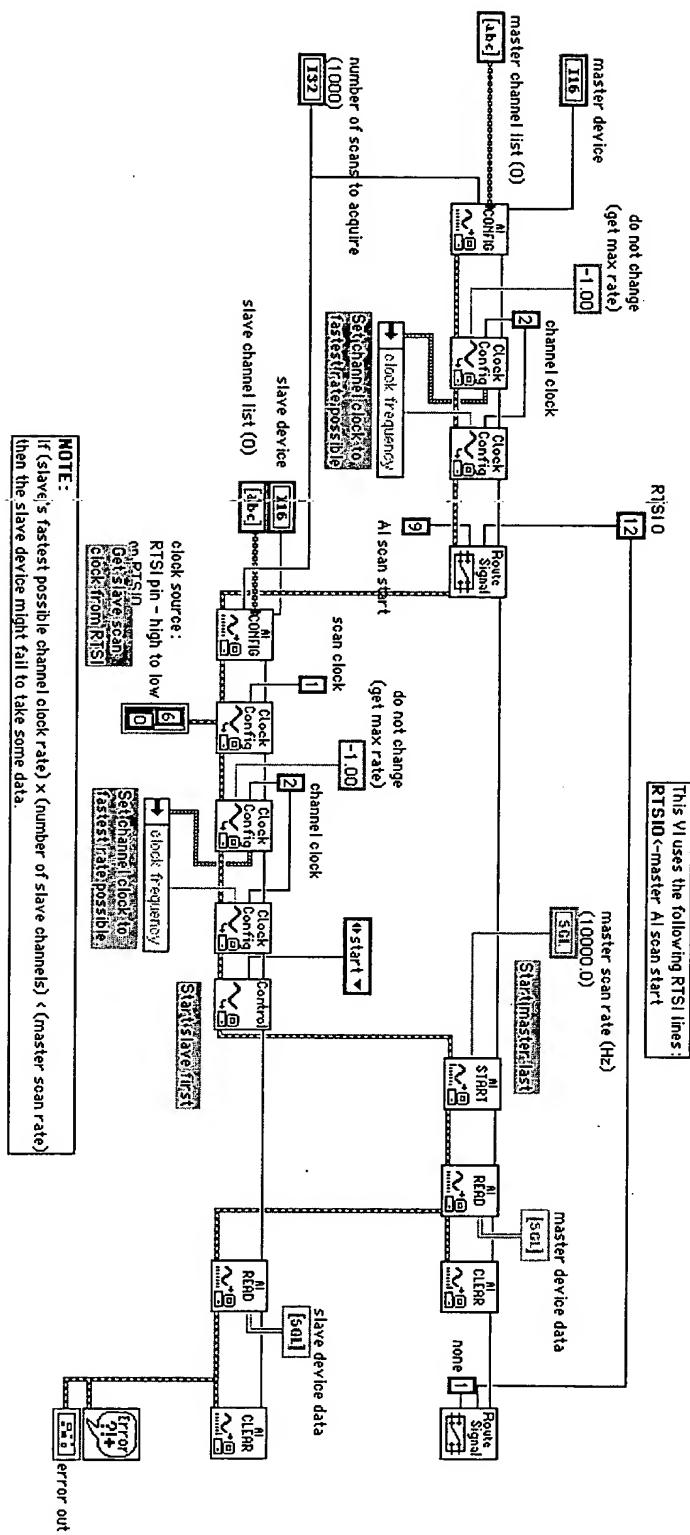
Simultaneous Triggered Buffered AI/AO (Prior Art)

Figure 40A



Simultaneous Triggered Buffered AI/AO

Figure 40B



Sharing Scan Clock Across Two E-Series Devices (Prior Art)

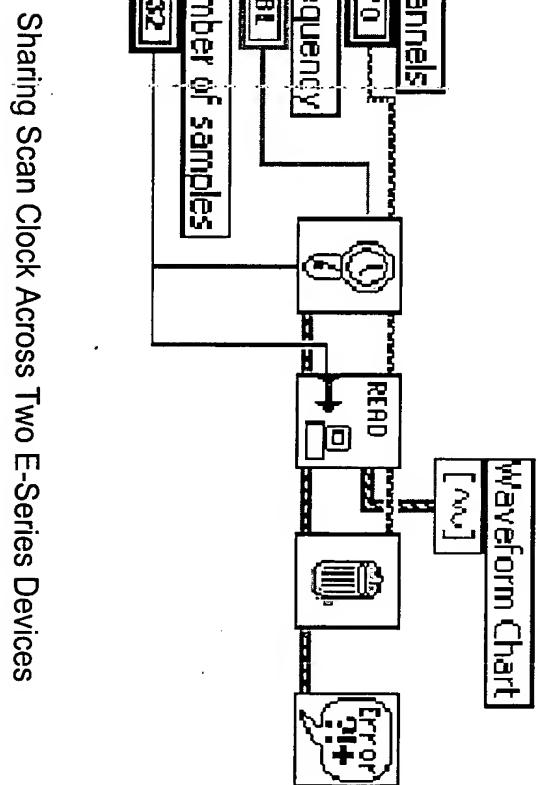
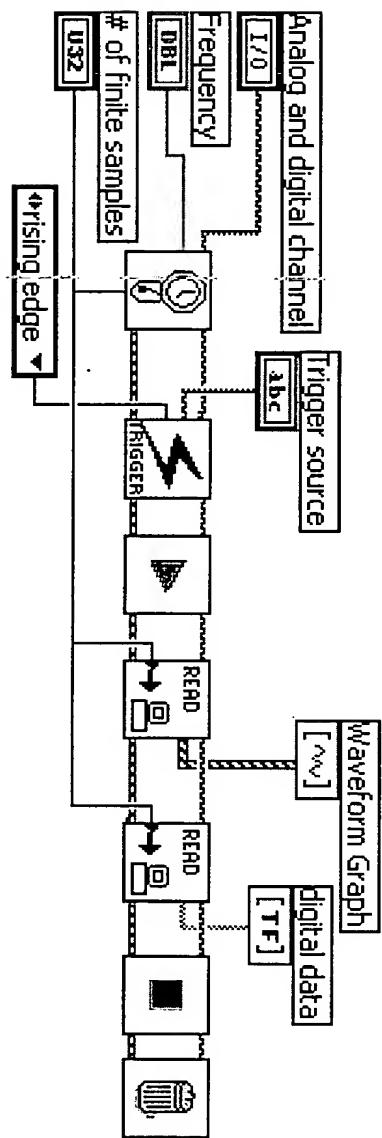


Figure 41B

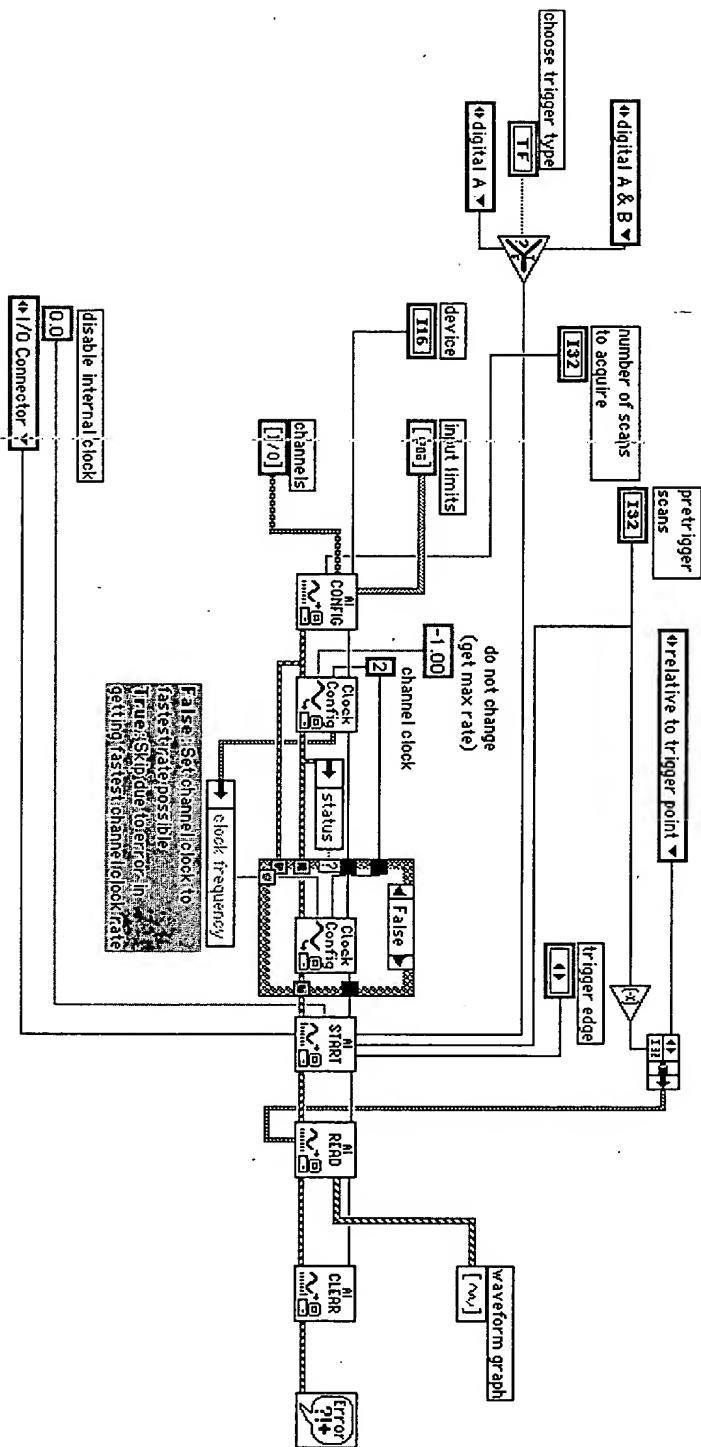


Sharing Clock And Trigger, Buffered AI & DI

Figure 42

Figure 43A (Prior Art)

Acquire N Scans External Scan Clock Digital Trigger (Prior Art)



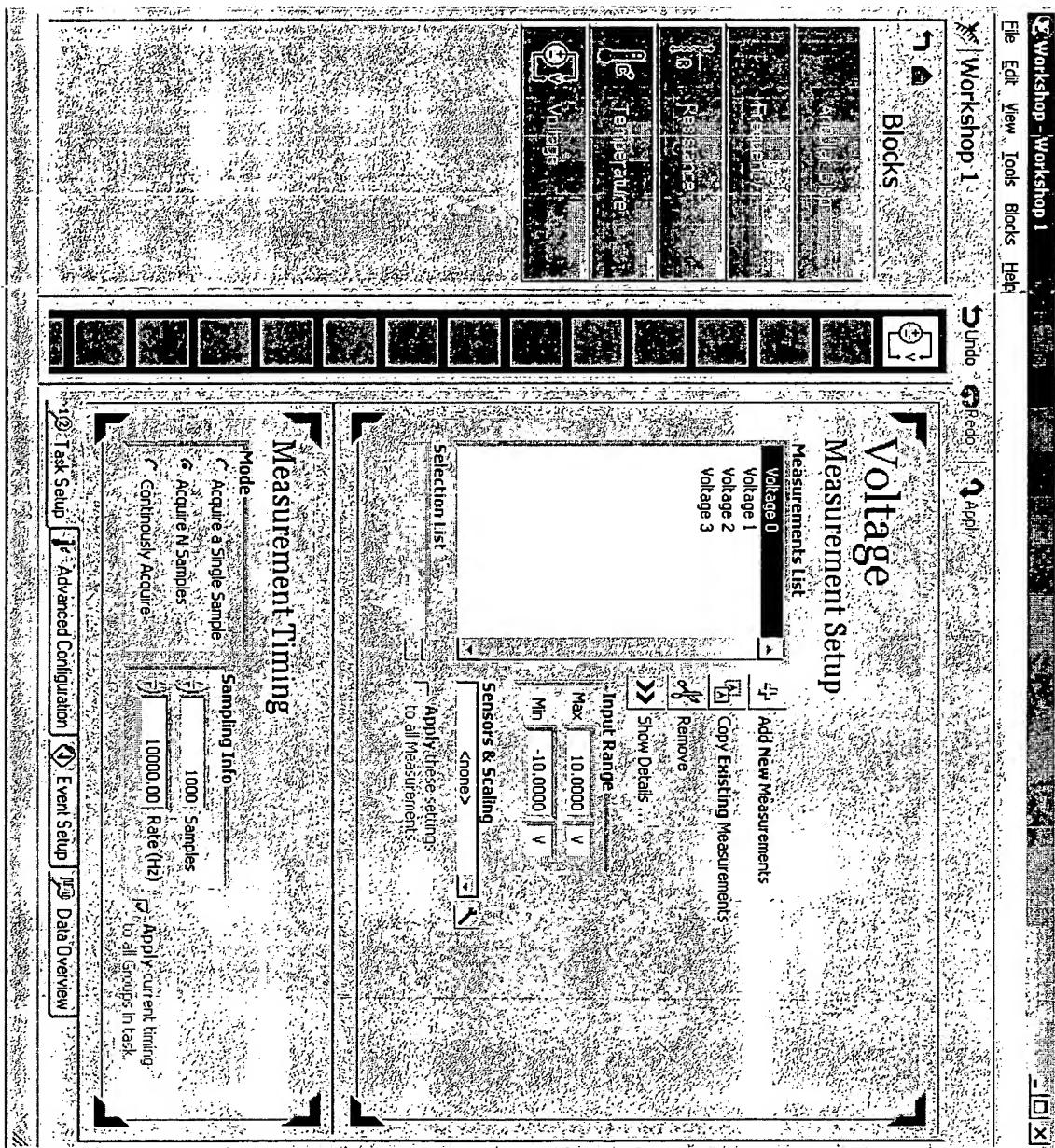


Figure 43B

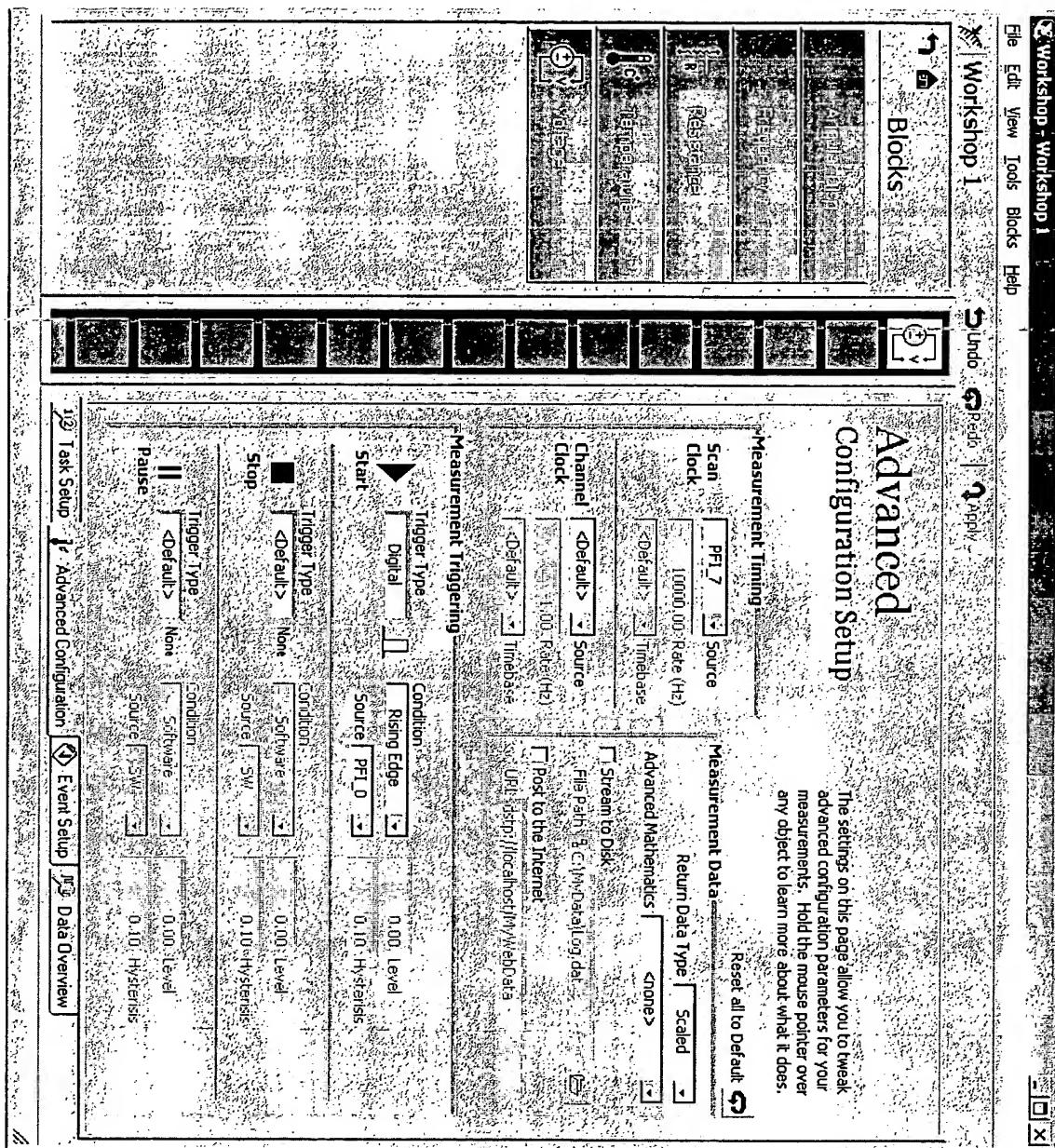
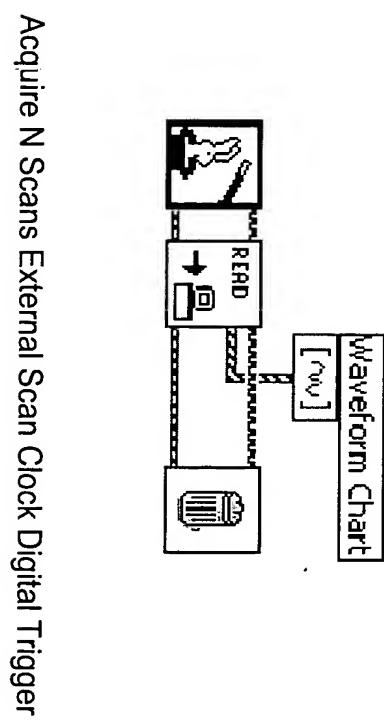


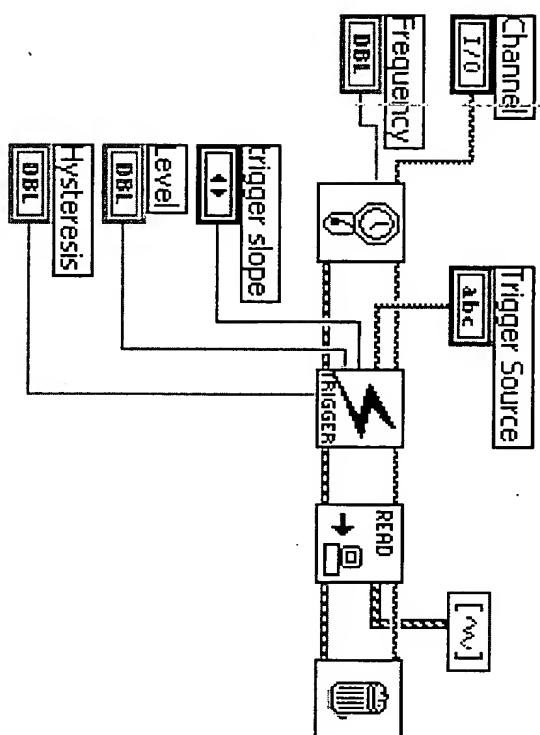
Figure 43C



Acquire N Scans External Scan Clock Digital Trigger

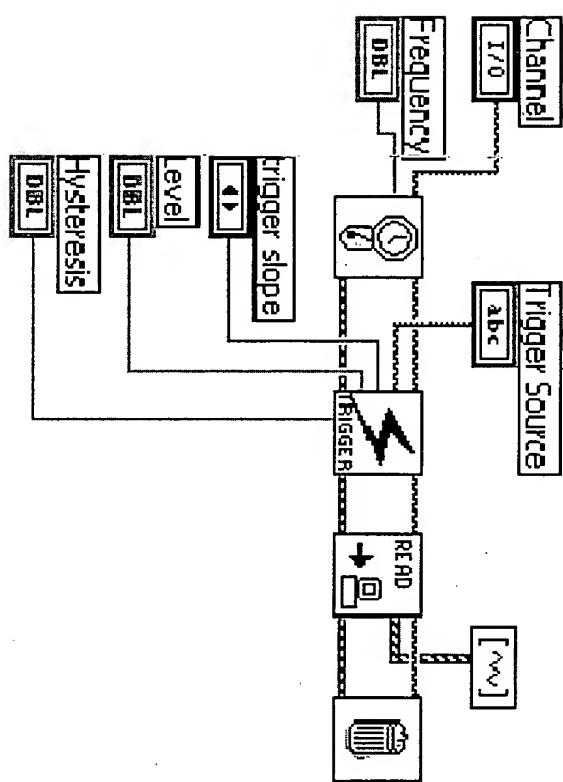
Figure 43D

100-240VAC 50/60Hz



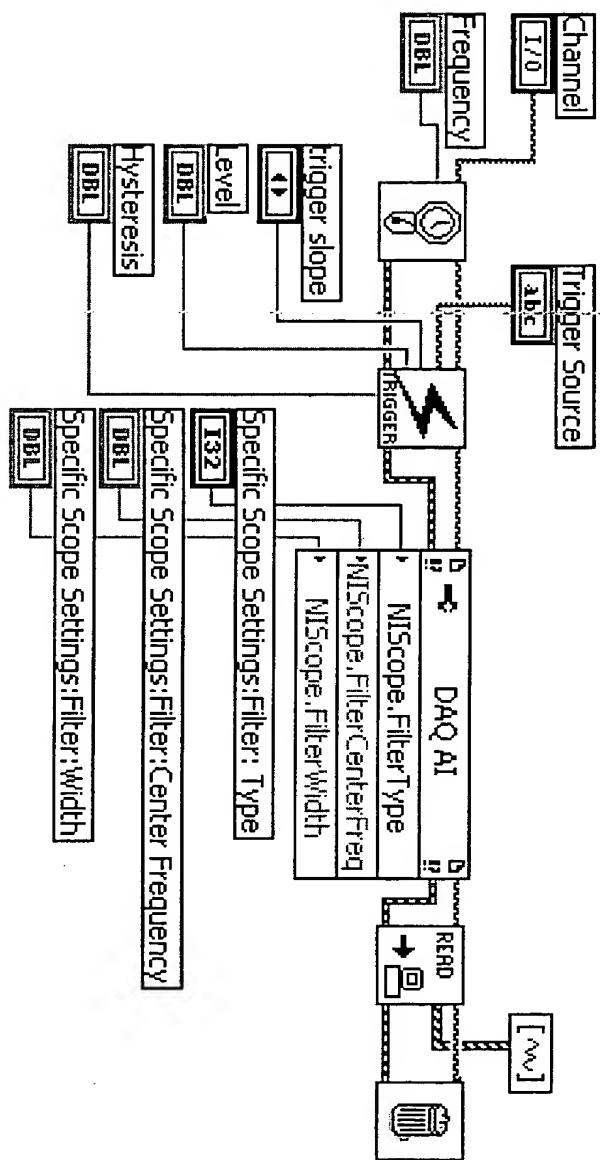
Triggered Acquisition With E-Series Device

Figure 44A



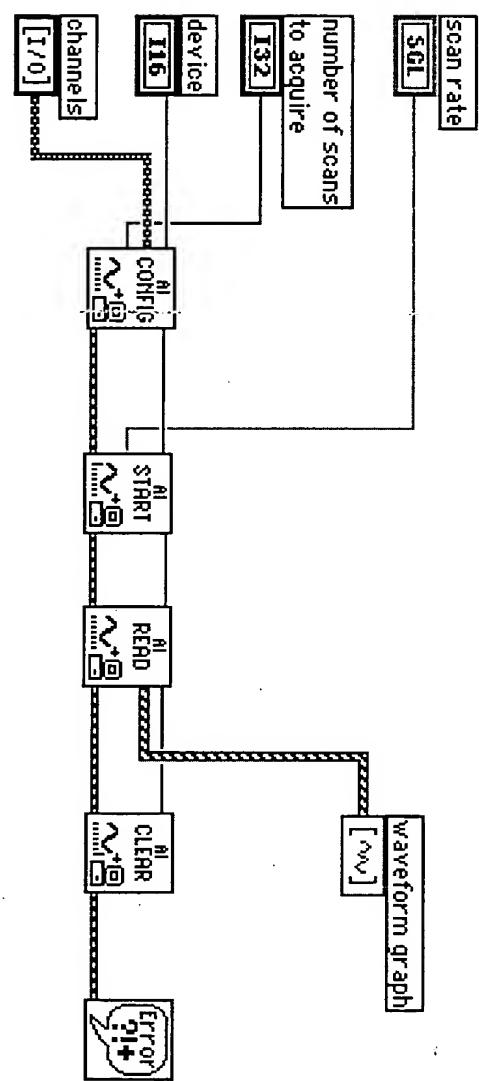
Triggered Acquisition With High Speed Digitizer

Figure 44B



Triggered Acquisition With High Speed Digitizer With Filtering

Figure 44C

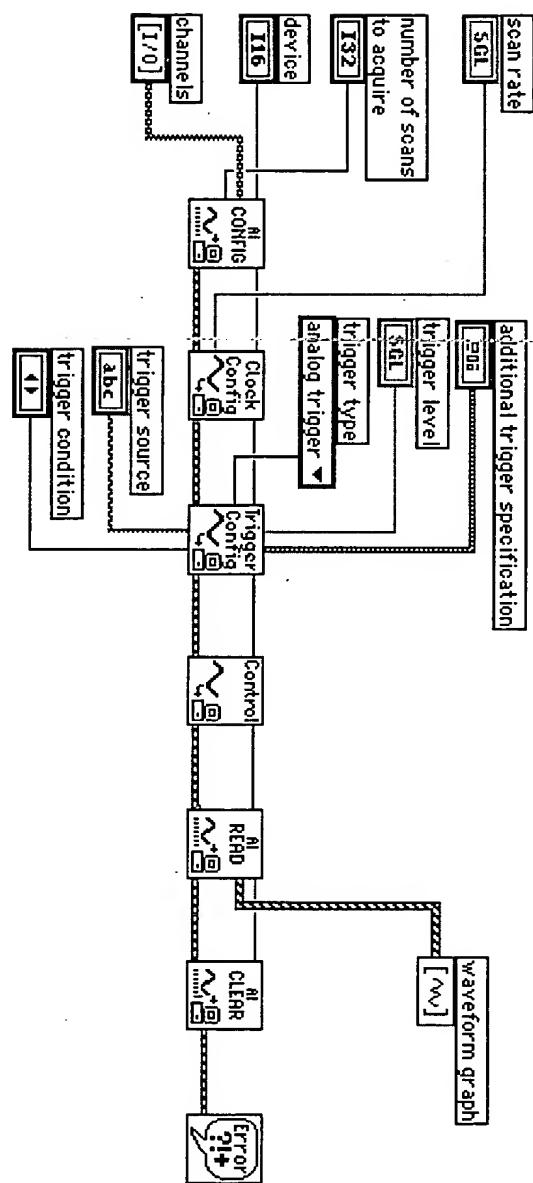


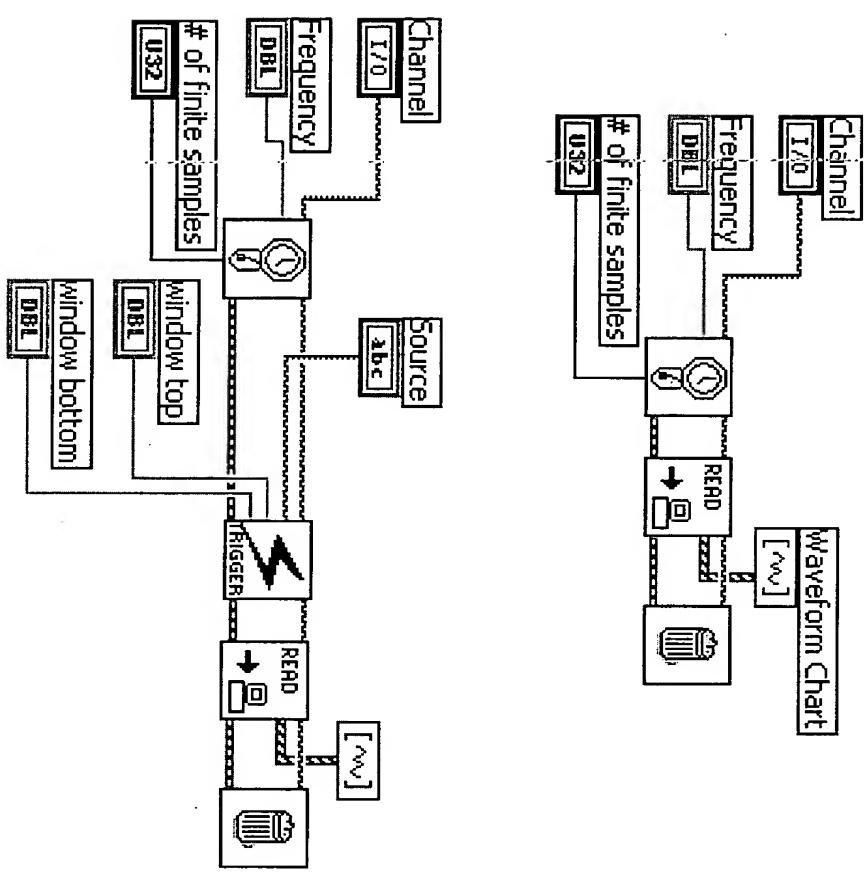
Intermediate Layer (Prior Art)

Figure 45A

Figure 45B

Changes For Analog Window Triggering (Prior Art)





Analog Window Triggering

Figure 45C